

Compal Confidential

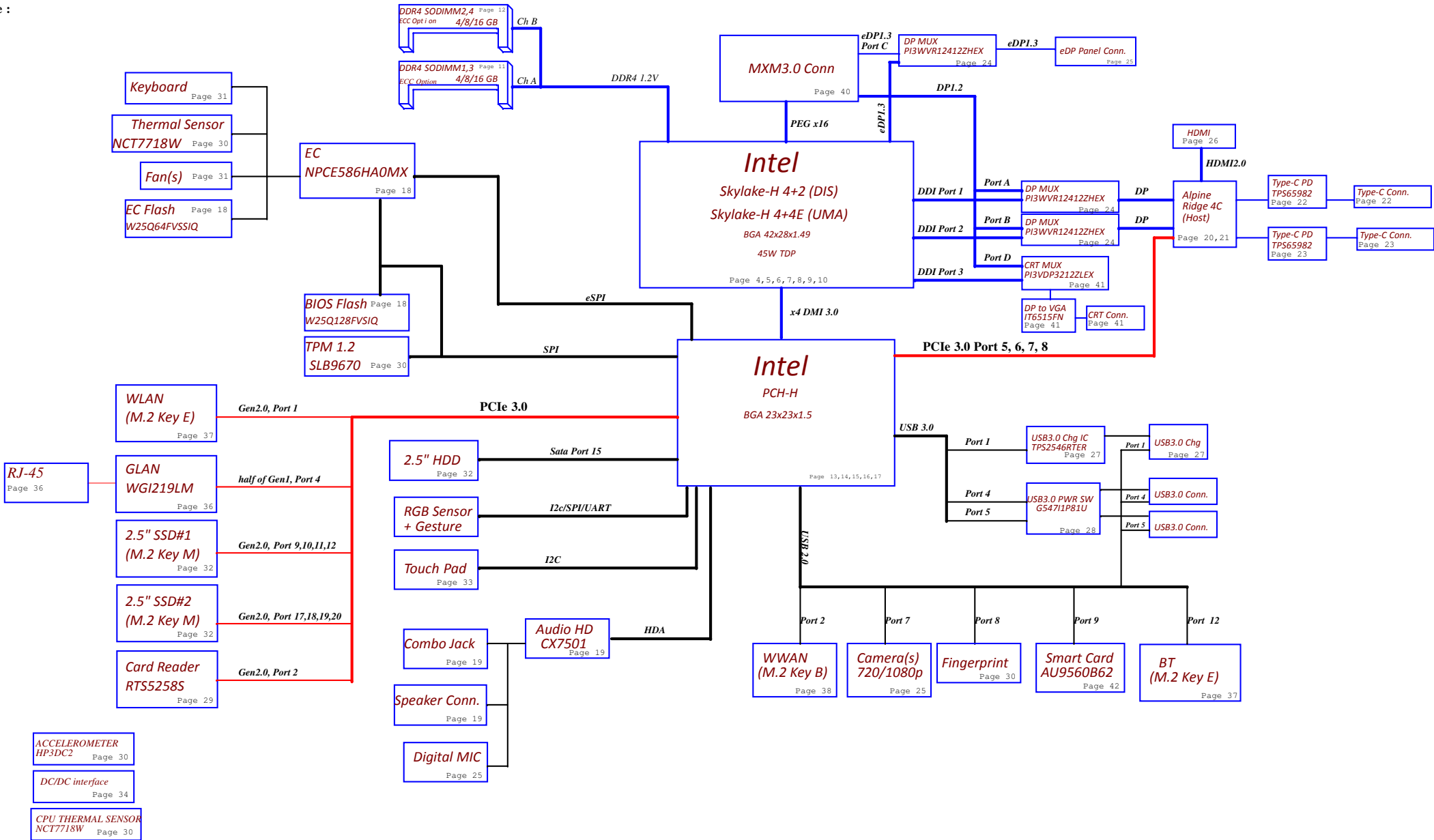
Intel Skylake-H 4+4e Processor with SPT-H_PCH

Venetian MXM

Date : 2016/03/08

Version 0.2

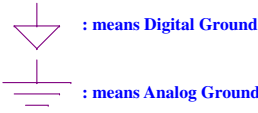
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/03/07	Deciphered Date	2018/03/07	Title	
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Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VDS +3VDS +1VALW +1.8VALW	+2.5V +1.2V_VDDQ +0.6VS_VTT	+5VS +3VS +VCC_CORE +VCC_GT +VCC_SA	
S0	0	0	0	0	0	
S1	0	0	0	0	0	
S3	0	0	0	0	X	
S5 S4/AC	0	0	0	X	X	
S5 S4/ Battery only	0	0	X	X	X	
S5 S4/AC & Battery don't exist	0	X	X	X	X	

Symbol Note :



@ : means just reserve , no build

CONN@ : means ME part.



Install below 45 level BOM structure for ver. 0.3

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.3

EMI@ : means just build for EMI's part
ESD@ : means just build for ESD's part
RF@ : means just build for RF's part
SSD@ : means just build for SSD part
HDD@ : means just build for HDD part
DB@ : means just build for Debug port part Remove before MP
H42@ : means just build for 4+2 CPU part
H44e@ : means just build for 4+4 CPU part
ESPI@ : means just build for eSPI interface part
LPC@ : means just build for LPC interface part

SMBUS Control Table

	SOURCE Embedded Controller	BATT	Therm Sensor 1001100xb	G-SENSOR 0101001xb	MXM	NIC 0x08	XDP	SODIMM	TP
I2C_MAIN_CLK I2C_MAIN_DATA	NPCE586	V	V	X	X	X	X	X	X
THERM_CLK THERM_DATA	NPCE586	X	X	X	V	X	X	X	X
PCH_KBC_CLK PCH_KBC_DATA	NPCE586	X	X	V	X	X	X	X	X
NIC_SMCLK NIC_SMDAT	Skylake	X	X	X	X	V	X	X	X
SMBUS_CLK SMBUS_DATA	Skylake	X	X	X	X	X	V	V	V

Stapping Options PLT_ID

PLT_ID0	PLT_ID1	PLT_ID2	SKU
0	0	0	
0	0	1	
0	1	0	
0	1	1	17W
1	0	0	
1	0	1	15W
1	1	0	
1	1	1	15U

CFG for AR HDMI SET

TBT_SRC_CFG1	HIGH	HDMI Mode
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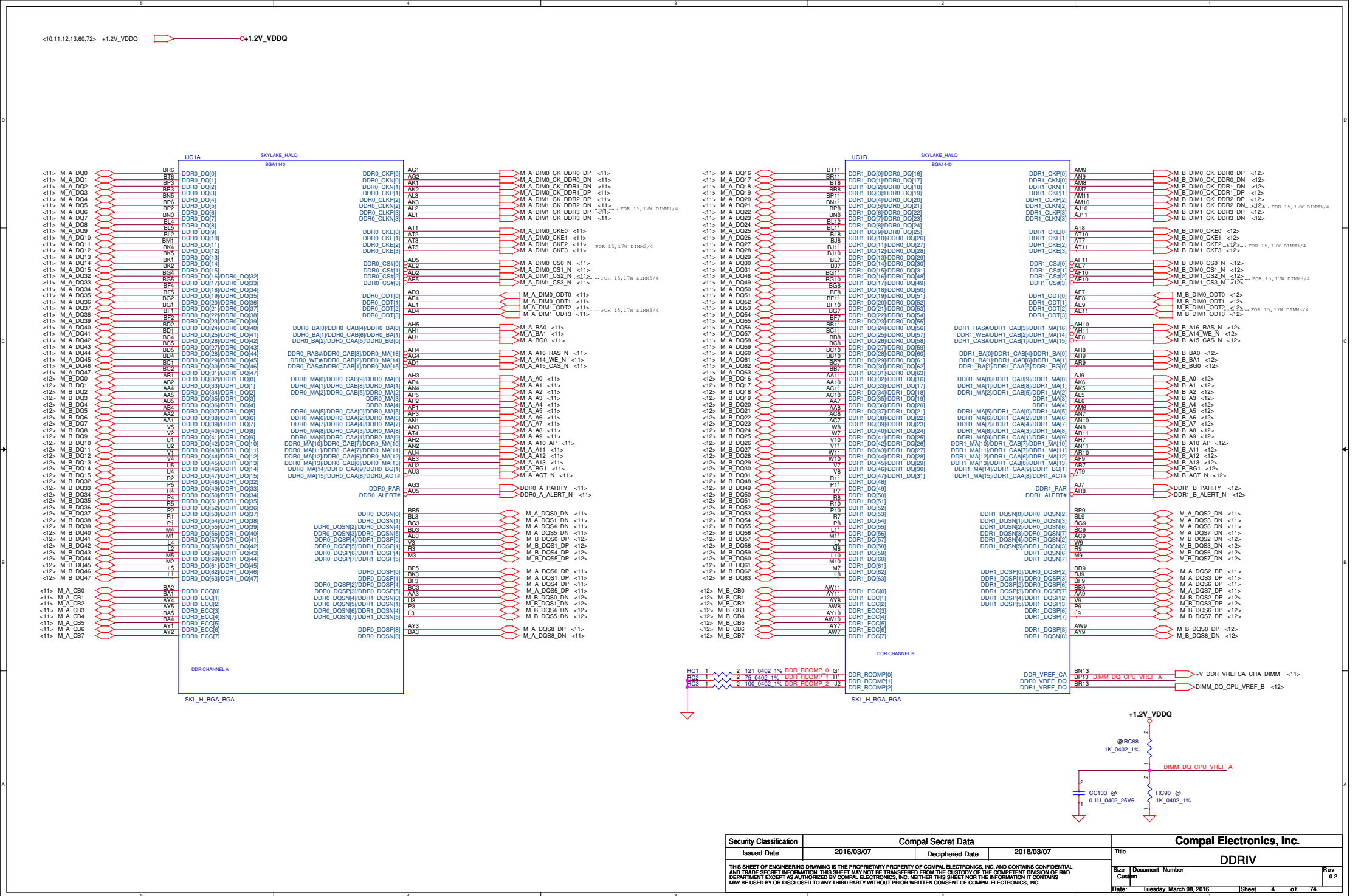
LE1	LE2	MODE	NOTE
V	X	LPC	
X	V	ESPI	

Stapping Options Flash

GPIO 51 Bit 1	GPIO 19 Bit 0	Boot BIOS Destination
0	0	Reserved
0	1	RSVD
1	0	SPI
1	1	LPC

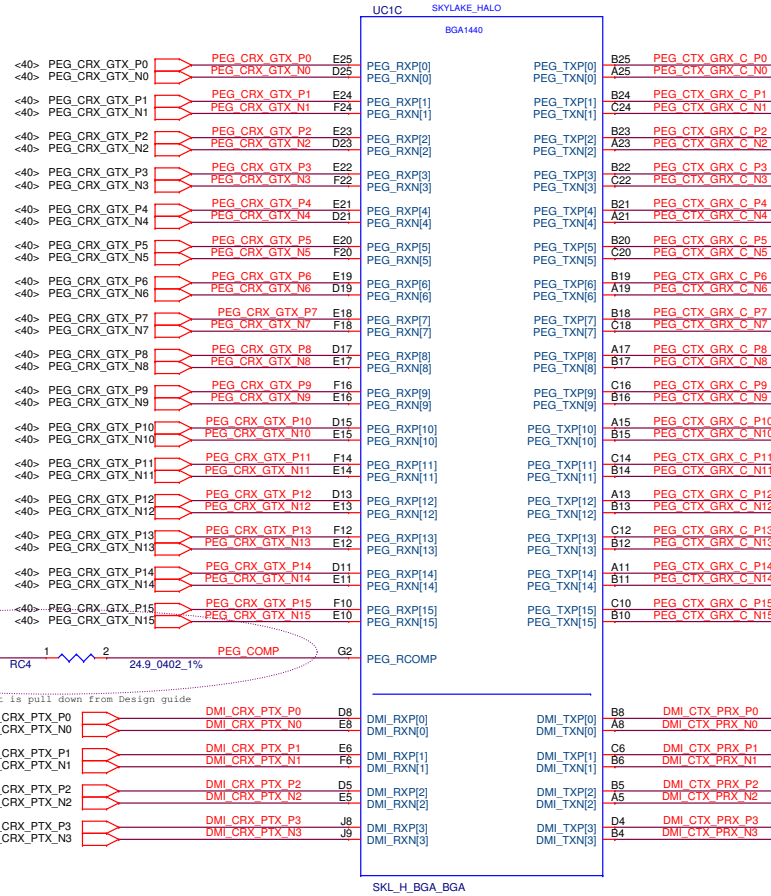
LPC & ESPI TABLE			
	LPC MODE	ESPI MODE	PAGE
RH371	0 OHM	15 OHM	13
RH372	0 OHM	15 OHM	
RH373	0 OHM	15 OHM	
RH374	0 OHM	15 OHM	
RH335	INSTALL	UNINSTALL	
RH368	INSTALL	UNINSTALL	
RH265	INSTALL	UNINSTALL	
RH369	INSTALL	UNINSTALL	
RH370	INSTALL	UNINSTALL	
RH198	INSTALL	UNINSTALL	
RH292	UNINSTALL	INSTALL	
RH275	INSTALL	UNINSTALL	
RH117	INSTALL	UNINSTALL	
RH376	INSTALL	UNINSTALL	15
RH109	UNINSTALL	INSTALL	
RH375	UNINSTALL	INSTALL	
RH274	UNINSTALL	INSTALL	
RH243	INSTALL	UNINSTALL	16
RH165	INSTALL	UNINSTALL	17
RH168	UNINSTALL	INSTALL	
LE1	INSTALL	UNINSTALL	18
LE2	UNINSTALL	INSTALL	
RE151	INSTALL	UNINSTALL	
RE130	INSTALL	UNINSTALL	
RE131	UNINSTALL	INSTALL	
RE89	UNINSTALL	INSTALL	
RE90	INSTALL	UNINSTALL	
RE152	INSTALL	UNINSTALL	
RE4	UNINSTALL	INSTALL	
RE144	UNINSTALL	INSTALL	

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2016/03/07		2018/03/07		Title	
2018/03/07		2018/03/07		Note List	
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<6,7,10,31,63> +VCC_IO



PEG_CTX_GRX_P[0..15] PEG_CTX_GRX_P[0..15] <40>
PEG_CTX_GRX_N[0..15] PEG_CTX_GRX_N[0..15] <40>

PEG_CTX_GRX_C_P0	CC2	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_P0
PEG_CTX_GRX_C_N0	CC3	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_N0
PEG_CTX_GRX_C_P1	CC4	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_P1
PEG_CTX_GRX_C_N1	CC5	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_N1
PEG_CTX_GRX_C_P2	CC6	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_P2
PEG_CTX_GRX_C_N2	CC7	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_N2
PEG_CTX_GRX_C_P3	CC8	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_P3
PEG_CTX_GRX_C_N3	CC9	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_N3
PEG_CTX_GRX_C_P4	CC10	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_P4
PEG_CTX_GRX_C_N4	CC11	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_N4
PEG_CTX_GRX_C_P5	CC12	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_P5
PEG_CTX_GRX_C_N5	CC13	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_N5
PEG_CTX_GRX_C_P6	CC14	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_P6
PEG_CTX_GRX_C_N6	CC15	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_N6
PEG_CTX_GRX_C_P7	CC16	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_P7
PEG_CTX_GRX_C_N7	CC17	2	1	0.22u	0201	6.3V	PEG_CTX_GRX_N7
PEG_CTX_GRX_C_P8	CC18	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_P8
PEG_CTX_GRX_C_N8	CC19	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_N8
PEG_CTX_GRX_C_P9	CC20	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_P9
PEG_CTX_GRX_C_N9	CC21	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_N9
PEG_CTX_GRX_C_P10	CC22	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_P10
PEG_CTX_GRX_C_N10	CC23	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_N10
PEG_CTX_GRX_C_P11	CC24	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_P11
PEG_CTX_GRX_C_N11	CC25	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_N11
PEG_CTX_GRX_C_P12	CC26	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_P12
PEG_CTX_GRX_C_N12	CC27	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_N12
PEG_CTX_GRX_C_P13	CC28	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_P13
PEG_CTX_GRX_C_N13	CC29	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_N13
PEG_CTX_GRX_C_P14	CC30	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_P14
PEG_CTX_GRX_C_N14	CC31	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_N14
PEG_CTX_GRX_C_P15	CC32	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_P15
PEG_CTX_GRX_C_N15	CC33	1	2	0.22u	0201	6.3V	PEG_CTX_GRX_N15

Layout Notes:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

+VCC_IO

PEG_COMP check list is pull down from Design guide

<14> DMI_CRX_PTX_P0	DMI_CRX_PTX_P0	D8	DMI_RXP[0]	DMI_TXP[0]	B8	DMI_CTX_PRX_P0	DMI_CTX_PRX_P0	<14>
<14> DMI_CRX_PTX_N0	DMI_CRX_PTX_N0	E8	DMI_RXN[0]	DMI_TXN[0]	A8	DMI_CTX_PRX_N0	DMI_CTX_PRX_N0	<14>
<14> DMI_CRX_PTX_P1	DMI_CRX_PTX_P1	F6	DMI_RXP[1]	DMI_TXP[1]	C6	DMI_CTX_PRX_P1	DMI_CTX_PRX_P1	<14>
<14> DMI_CRX_PTX_N1	DMI_CRX_PTX_N1	F6	DMI_RXN[1]	DMI_TXN[1]	B6	DMI_CTX_PRX_N1	DMI_CTX_PRX_N1	<14>
<14> DMI_CRX_PTX_P2	DMI_CRX_PTX_P2	D5	DMI_RXP[2]	DMI_TXP[2]	B5	DMI_CTX_PRX_P2	DMI_CTX_PRX_P2	<14>
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<14> DMI_CRX_PTX_P3	DMI_CRX_PTX_P3	J8	DMI_RXP[3]	DMI_TXP[3]	D4	DMI_CTX_PRX_P3	DMI_CTX_PRX_P3	<14>
<14> DMI_CRX_PTX_N3	DMI_CRX_PTX_N3	J9	DMI_RXN[3]	DMI_TXN[3]	B4	DMI_CTX_PRX_N3	DMI_CTX_PRX_N3	<14>

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<5,7,10,31,63> +VCC_IO



+VCC_IO

For 15,17W CRT

For 15,17W CRT

<24> DDI1_TX0_DP
<24> DDI1_TX0_DN
<24> DDI1_TX1_DP
<24> DDI1_TX1_DN
<24> DDI1_TX2_DP
<24> DDI1_TX2_DN
<24> DDI1_TX3_DP
<24> DDI1_TX3_DN

<24> DPC1_AUX_DP
<24> DPC1_AUX_DN

<24> DDI2_TX0_DP
<24> DDI2_TX0_DN
<24> DDI2_TX1_DP
<24> DDI2_TX1_DN
<24> DDI2_TX2_DP
<24> DDI2_TX2_DN
<24> DDI2_TX3_DP
<24> DDI2_TX3_DN

<24> DDI2_AUX_DP
<24> DDI2_AUX_DN

<41> DDI3_TX0_DP
<41> DDI3_TX0_DN
<41> DDI3_TX1_DP
<41> DDI3_TX1_DN

<41> DDI3_AUX_DP
<41> DDI3_AUX_DN

K36
K37
J35
J34
H37
H36
J37
J38

D27
E27

H34
H33
F37
G38
F34
F35
E37
E36

F26
E26

C34
D34
B36
B34
F33
E33
C33
B33

A27
B27

UC1D SKYLAKE_HALO
BGA1440
SKL_H_BGA_BGA

DDI1_TXP[0]
DDI1_TXN[0]
DDI1_TXP[1]
DDI1_TXN[1]
DDI1_TXP[2]
DDI1_TXN[2]
DDI1_TXP[3]
DDI1_TXN[3]

DDI1_AUXP
DDI1_AUXN

DDI2_TXP[0]
DDI2_TXN[0]
DDI2_TXP[1]
DDI2_TXN[1]
DDI2_TXP[2]
DDI2_TXN[2]
DDI2_TXP[3]
DDI2_TXN[3]

DDI2_AUXP
DDI2_AUXN

DDI3_TXP[0]
DDI3_TXN[0]
DDI3_TXP[1]
DDI3_TXN[1]
DDI3_TXP[2]
DDI3_TXN[2]
DDI3_TXP[3]
DDI3_TXN[3]

DDI3_AUXP
DDI3_AUXN

PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO

EDP_TXP[0]
EDP_TXN[0]
EDP_TXP[1]
EDP_TXN[1]
EDP_TXP[2]
EDP_TXP[3]
EDP_TXN[3]

EDP_AUXP
EDP_AUXN

EDP_DISP_UTIL
EDP_RCOMP

EDP_D_TX0_DP
EDP_D_TX0_DN
EDP_D_TX1_DP
EDP_D_TX1_DN
EDP_D_TX2_DN
EDP_D_TX2_DP
EDP_D_TX3_DN
EDP_D_TX3_DP

DDSP_3_D_AUX_DP
DDSP_3_D_AUX_DN

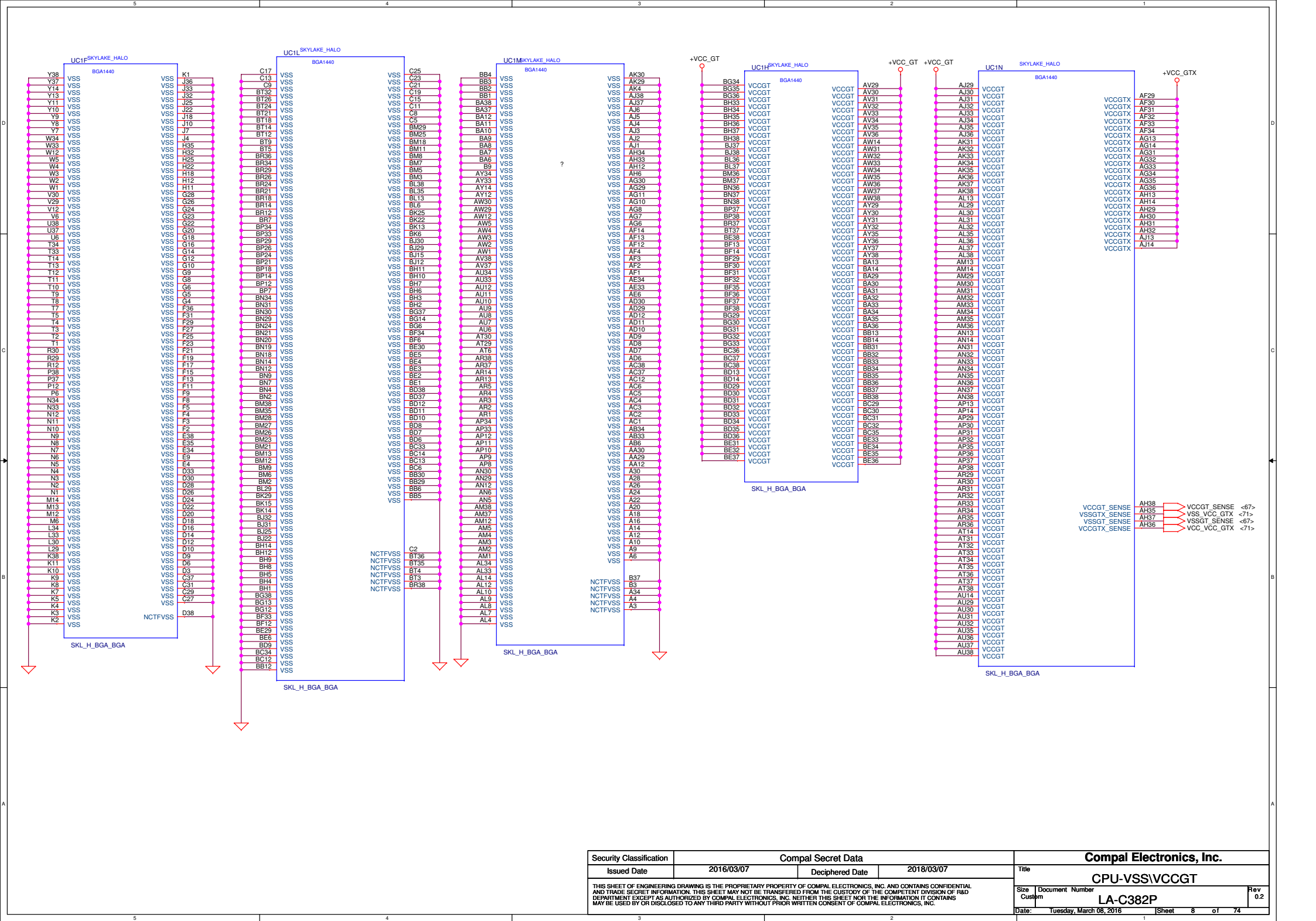
A33 EDP_DISP_UTIL @TP170 PAD
D37 EDP_COMP

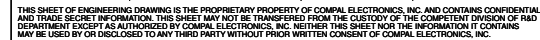
COMPENSATION PU FOR eDP
Layout Notes:
Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

AUD_AZACPU_R_SCLK
AUD_AZACPU_R_SDO
AUD_AZACPU_R_SDI

Vinafix.com

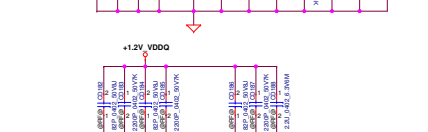
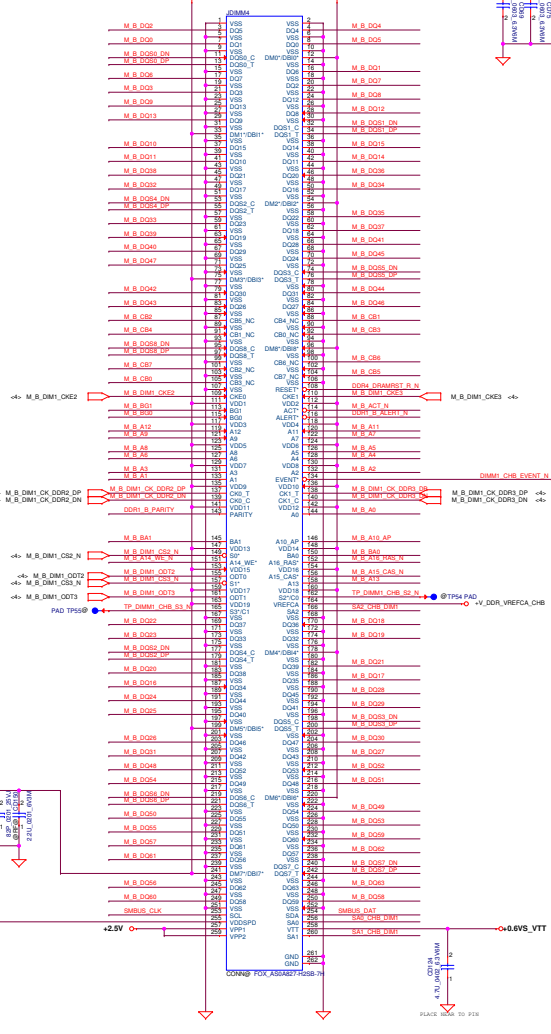
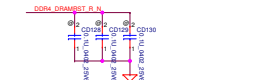
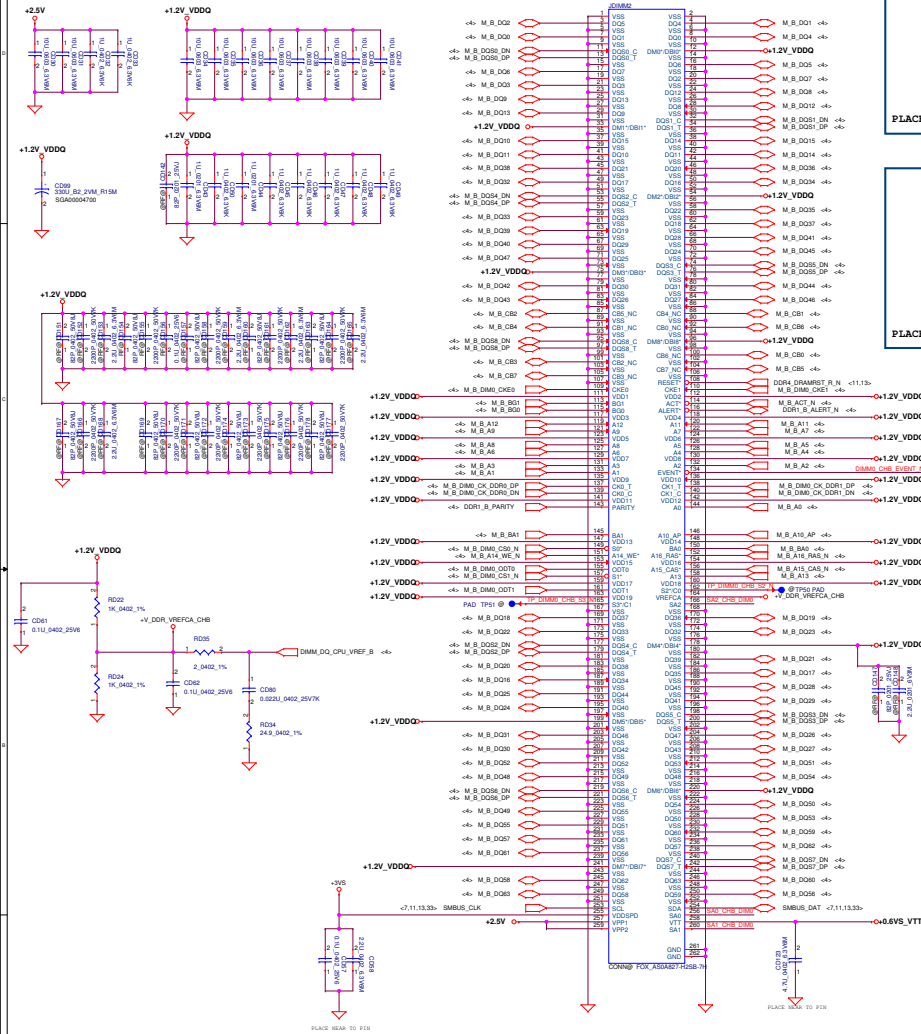
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Issued Date		2016/03/07	Deciphered Date	2018/03/07	Title	CPU-FDI,eDP,DDI			
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JDIMM1 H=4mm BOT

JDIMM4 H=9.2mm BOT



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Rev	D	Document Number	LA-C382P	Rev	6.1
Issue	1	Issued	2016/03/07	Drawn	12/07/16

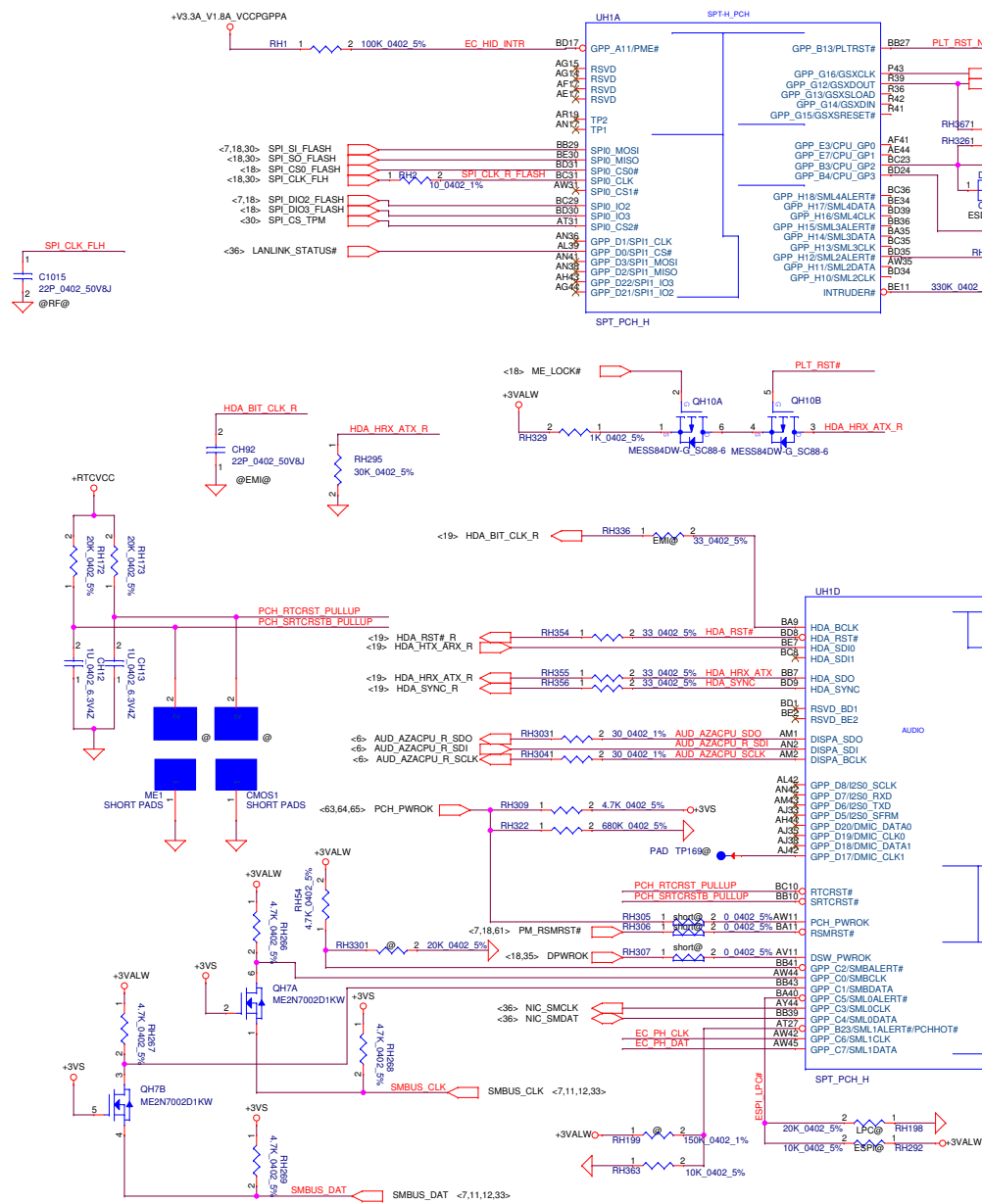
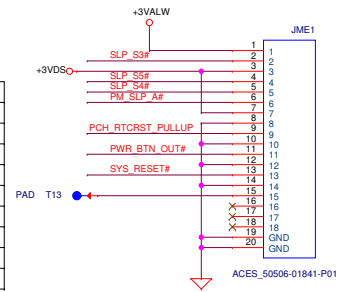
GPP_CS	Func.
HIGH	eSPI
LOW	LPC

ME Debug Port

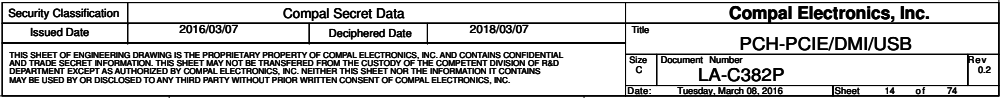
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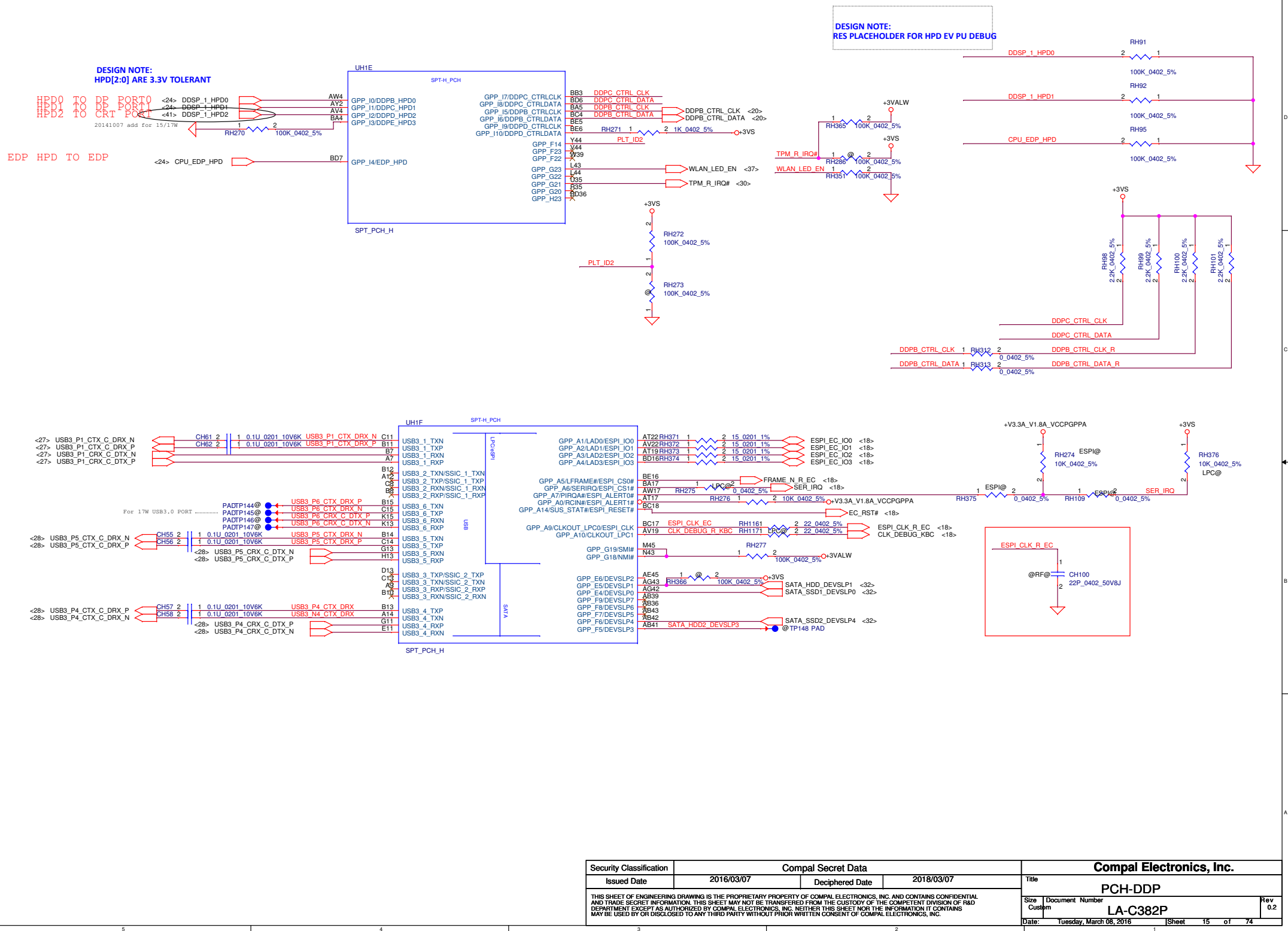
Pinout on customer's board, as in the PDG, CDI #546884

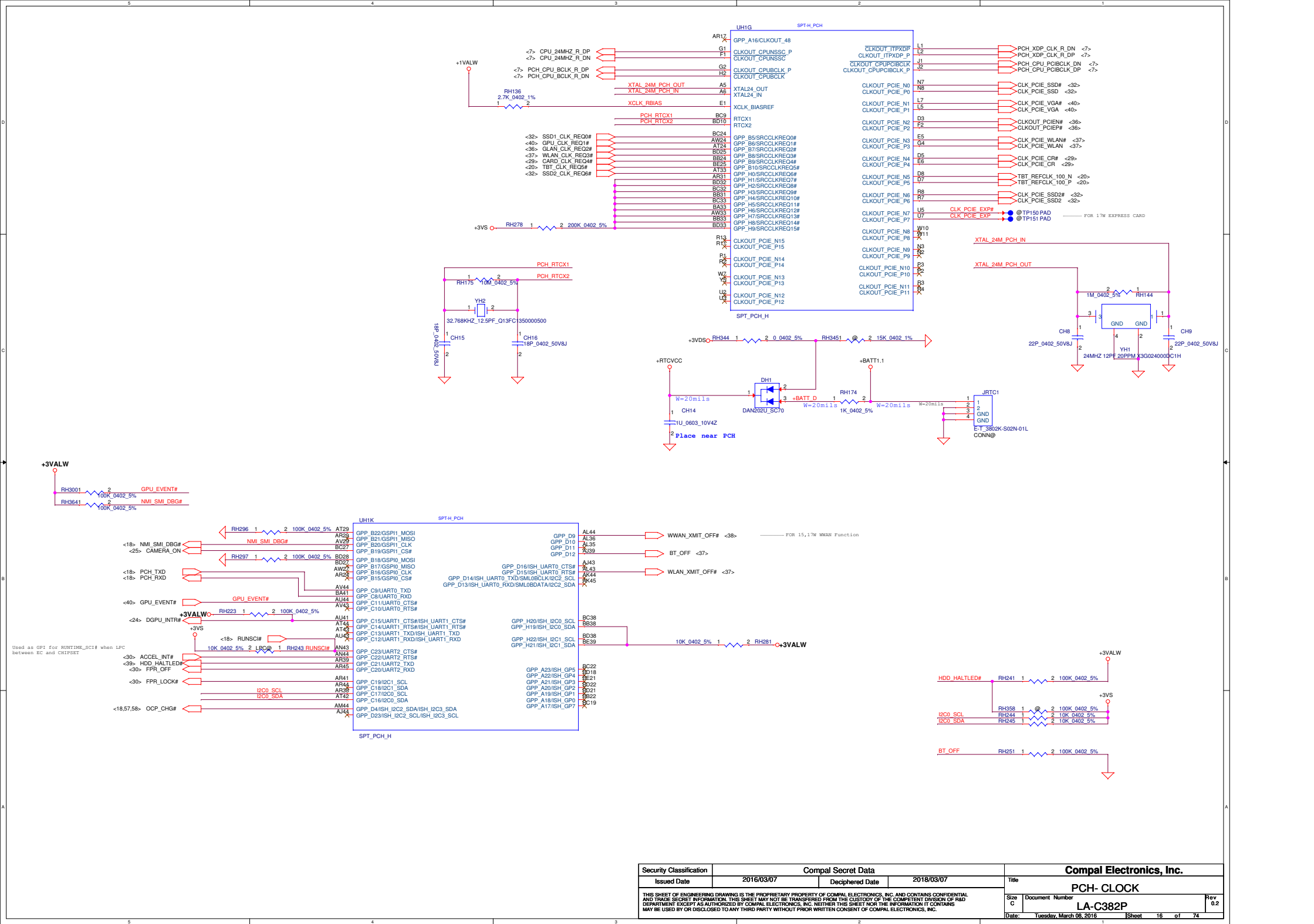
Pin	VccSus3_3	Pin	GND
1	SLEP_S3#	10	GND
2	SLEP_S3#	11	PWRBTN#
3	VccDSW3_3	12	GND
4	SLEP_S5#	13	SYS_RESET#
5	SLEP_S4#	14	GND
6	SLEP_A#	15	SLEP_S0#
7	+3.3DS	16	NC
8	GND	17	NC
9	RTRCRST#	14	NC

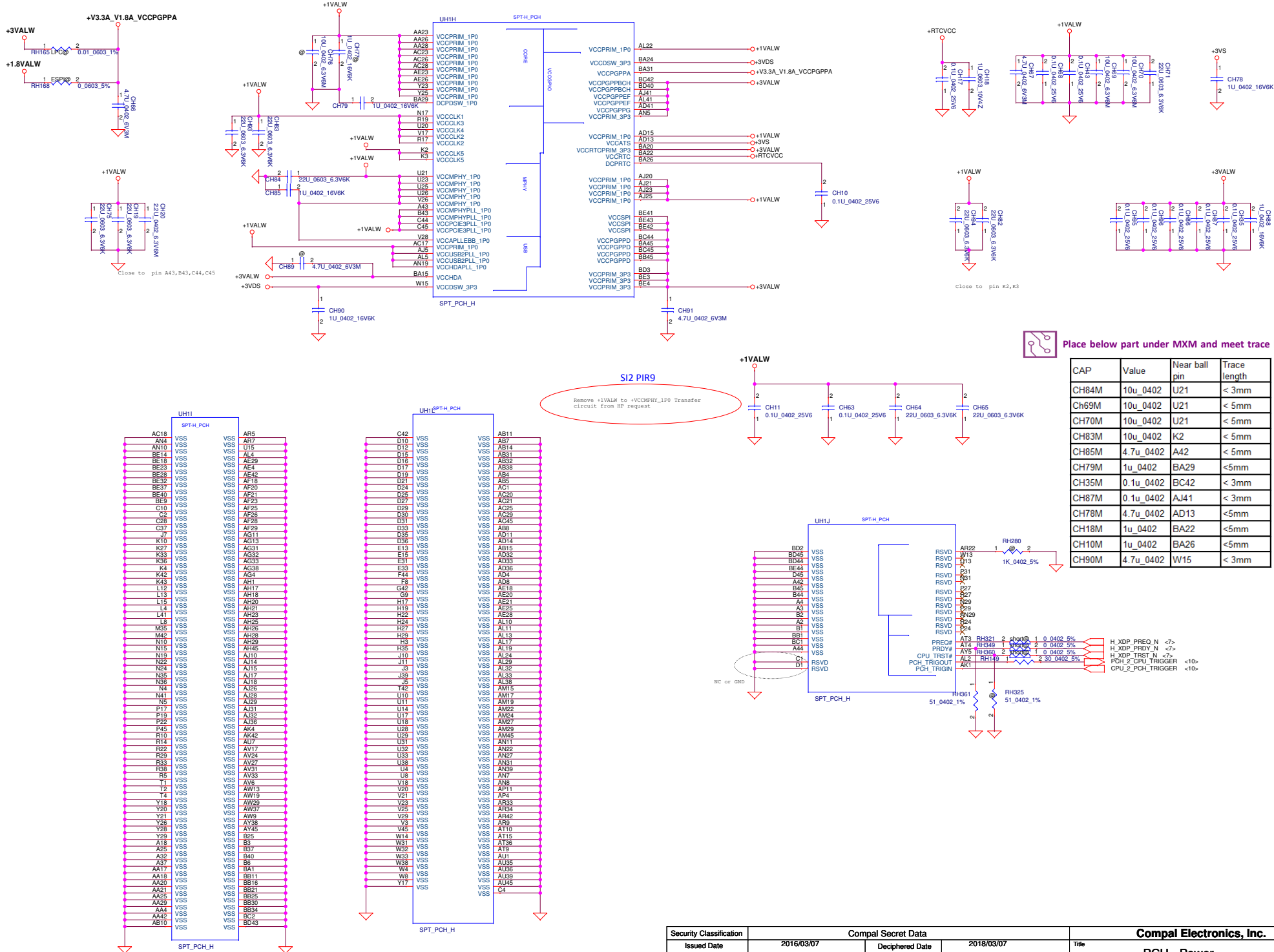


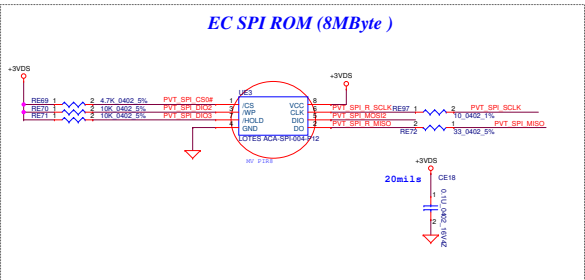
Security Classification	Compal Secret Data	Deciphered Date	2018/03/07	Title	PCH-SPI
Issued Date	2016/03/07	Deciphered Date	2018/03/07	Size	Document Number
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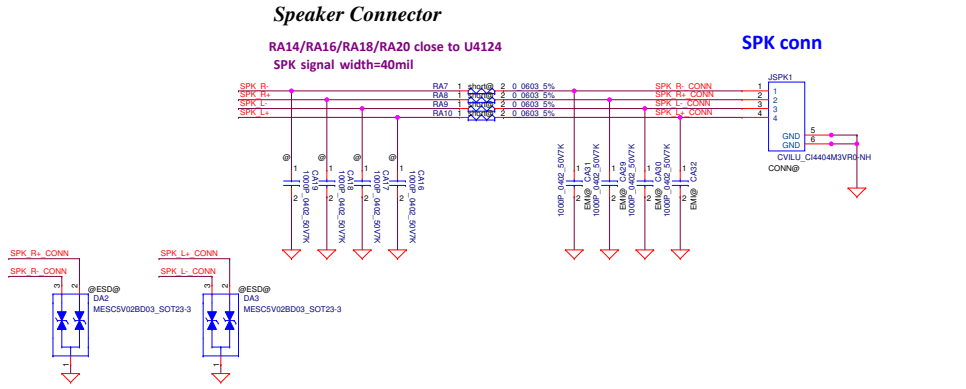
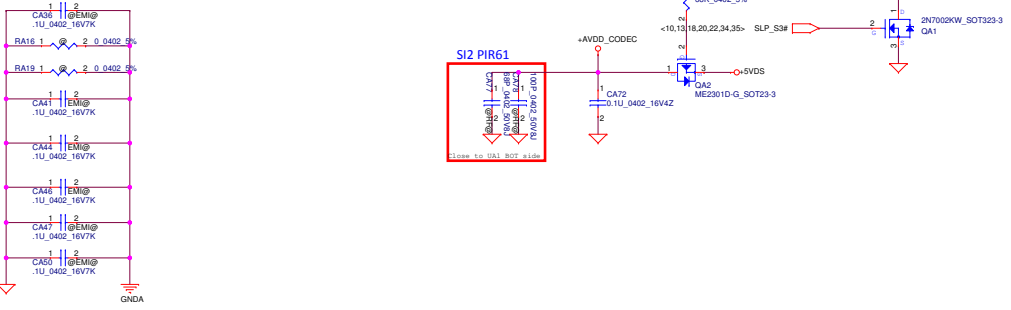
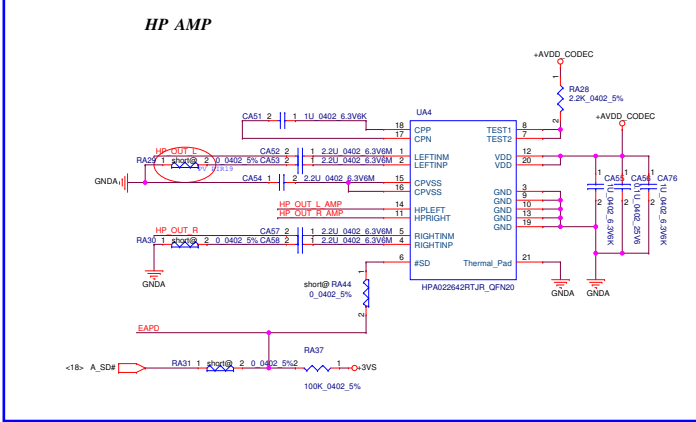
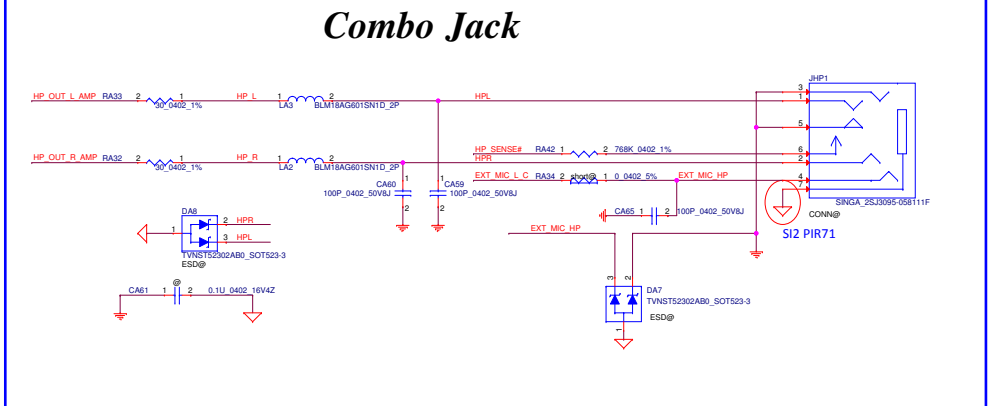
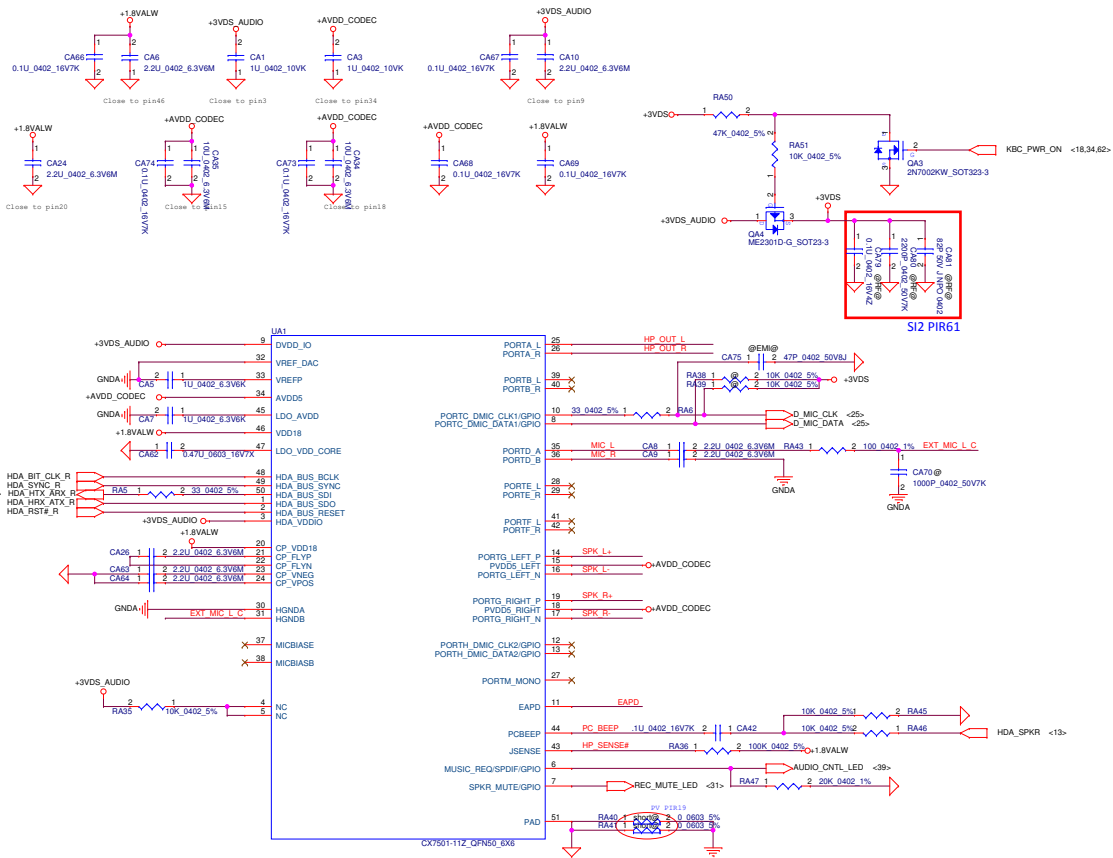




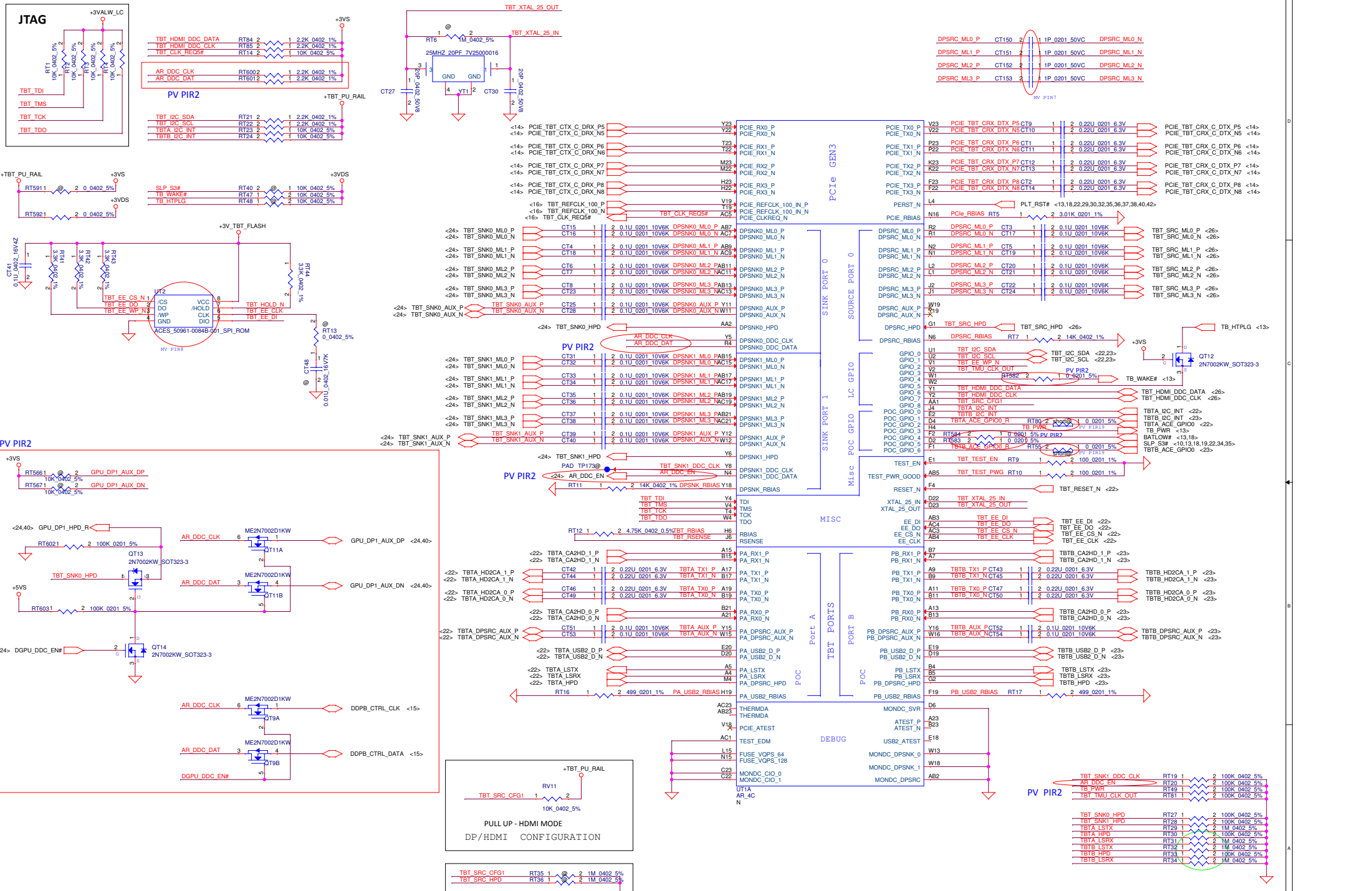


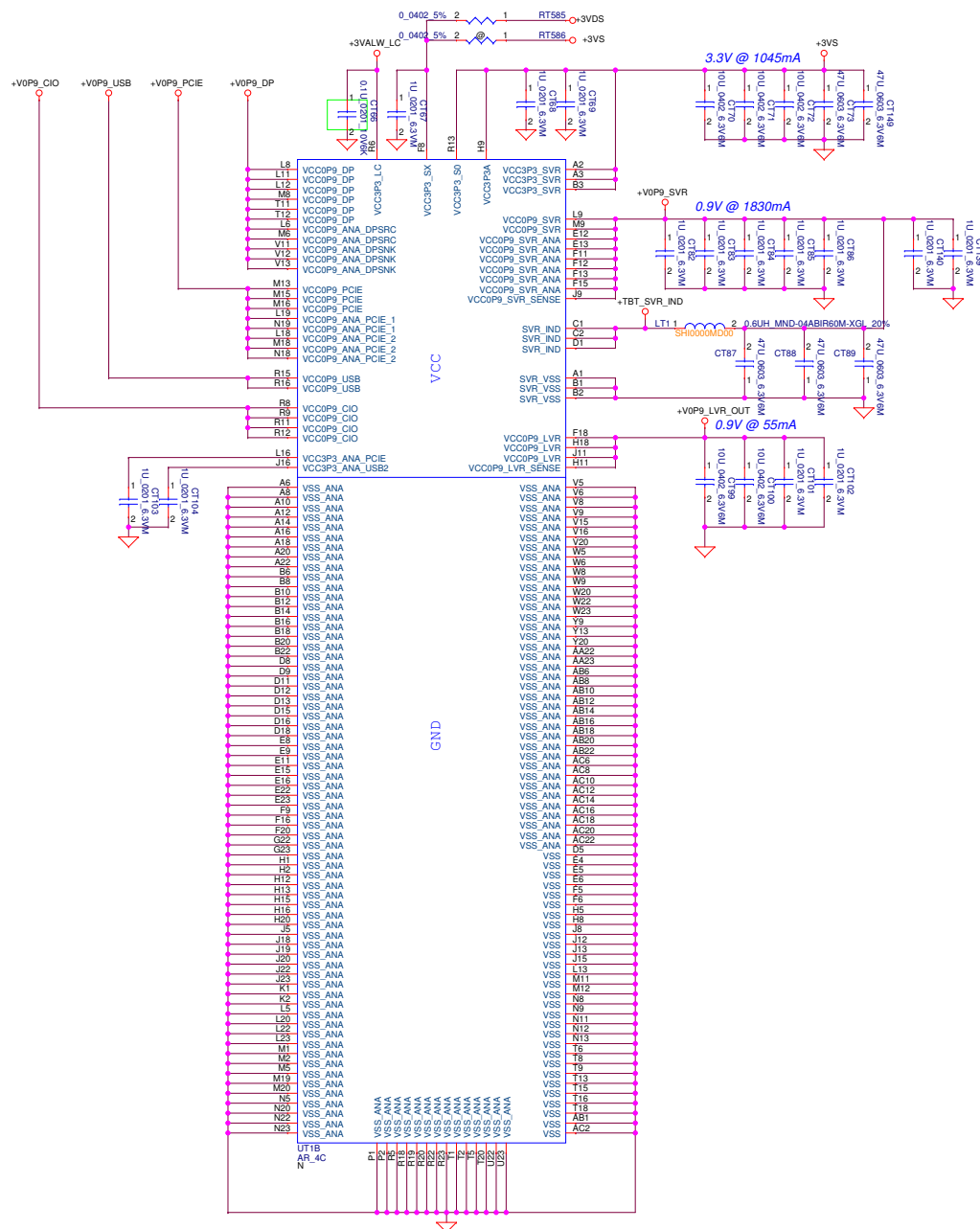
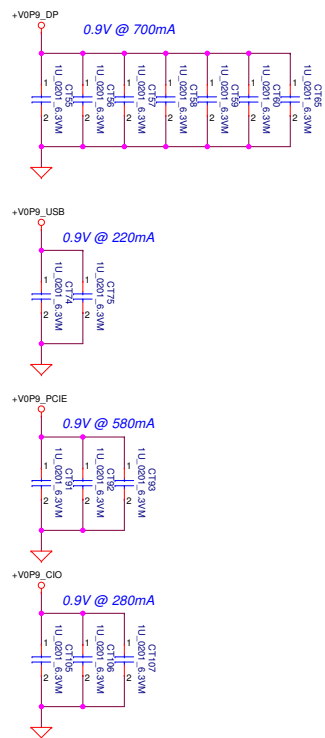






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Issued Date	2018/03/07	Deciphered Date	2018/03/07	Title	Audio codec CX20724
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				Date	LA-382P
				Drawn	Yuesday, March 06, 2018
				Sheet	19 of 24
				Rev	0.2



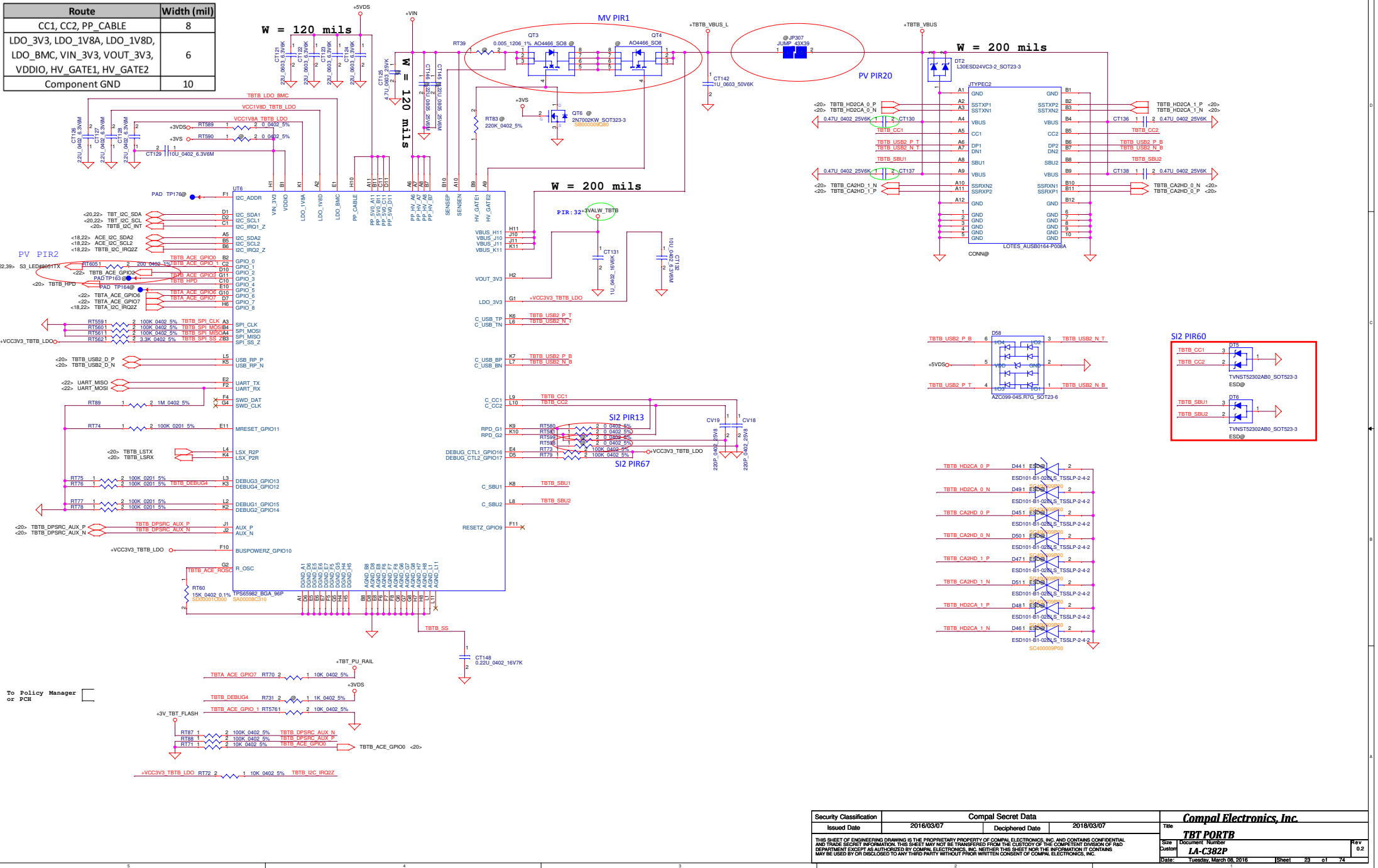


Route	Width (mil)
CC1, CC2, PP, CABLE	8
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Component GND	10

W = 120 mils

MV PIR1

W = 200 mils



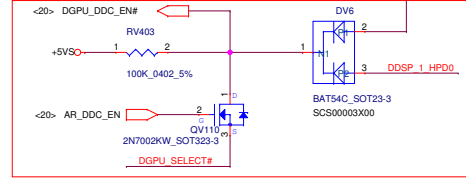
To Policy Manager
or PCH

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Issued Date	2016/03/07	Deciphered Date	2016/03/07	Title	TBT PORTB
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Size	Document Number	Date: Tuesday, March 08, 2016			Sheet 28 of 74

DP MUX

To AR

PV PIR2

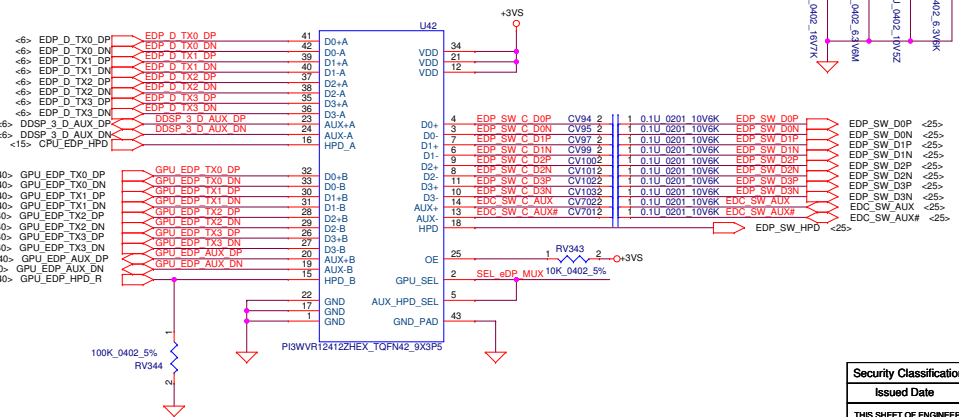


To AR

eDP MUX

From CPU

From GPU



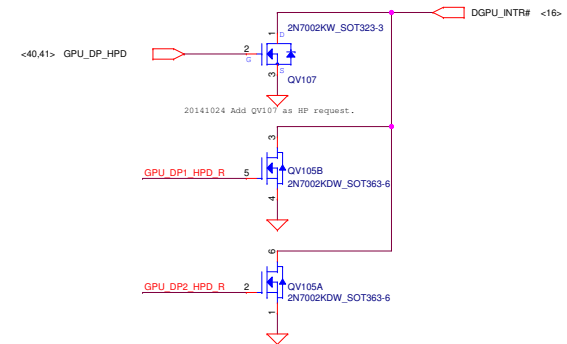
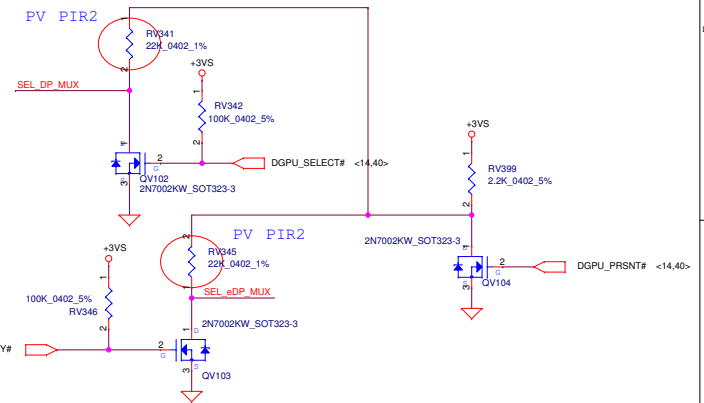
From CPU

From GPU

From CPU

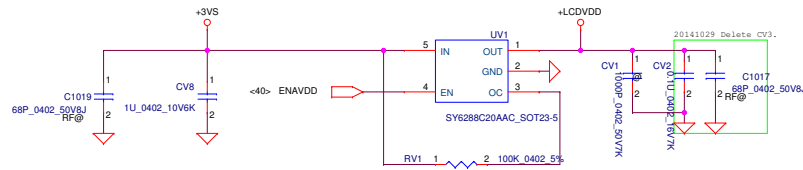
From GPU

To EDP Conn.

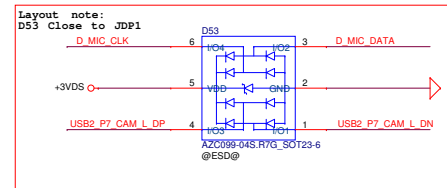
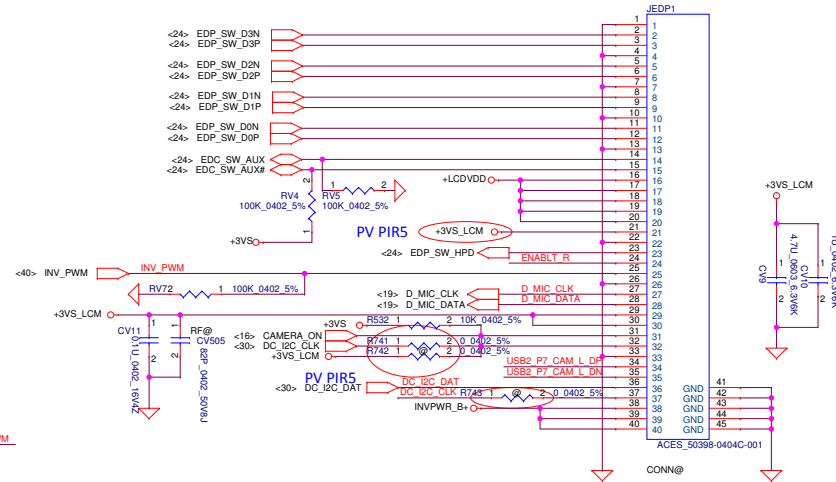
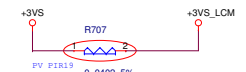
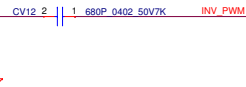
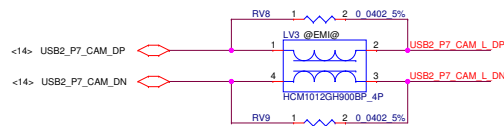
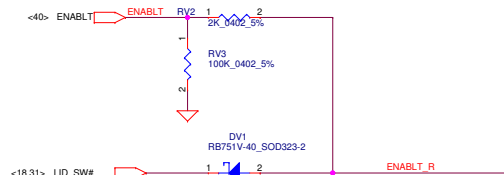
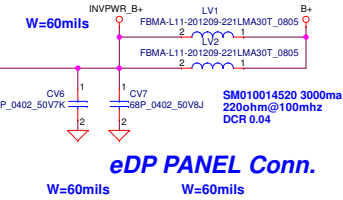
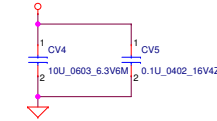


DGPU_SELECT#	UMA_ONLY#	Mode option
1	0	Invalid config
0	1	HP Hybrid SG
0	0	DGPU only
1	1	UMA/Headless SG

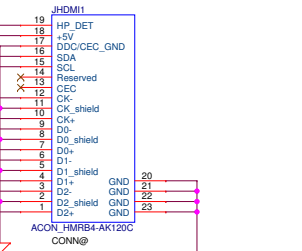
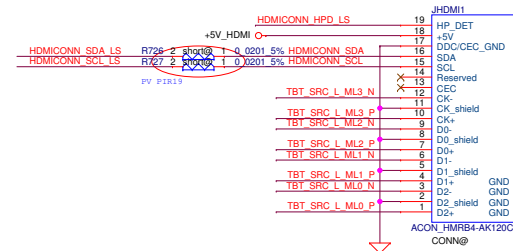
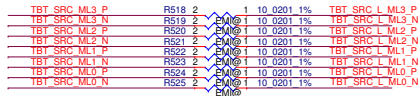
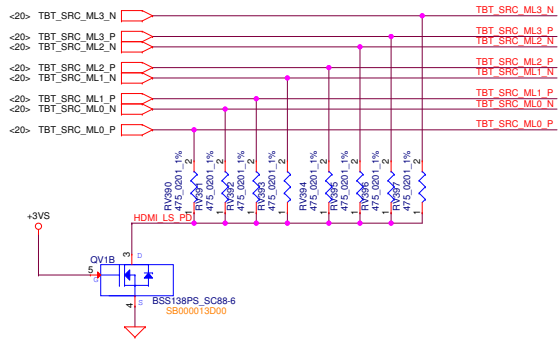
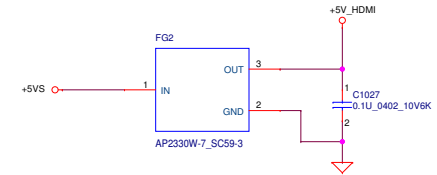
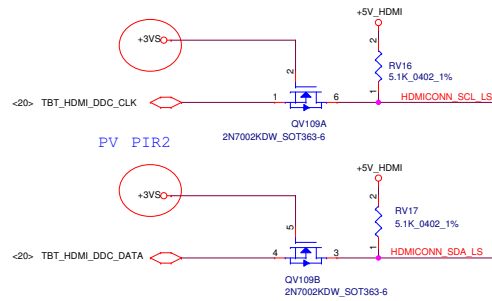
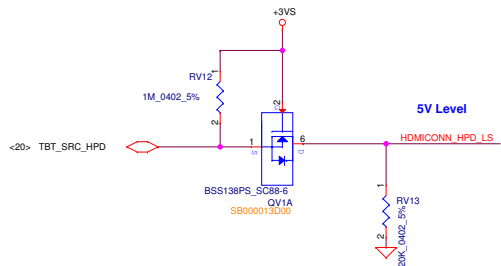
LCD POWER CIRCUIT



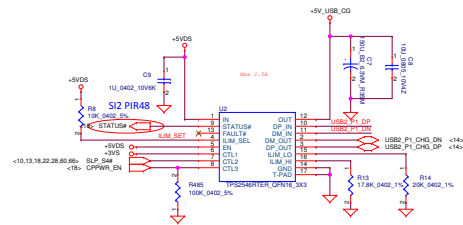
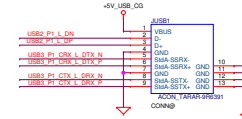
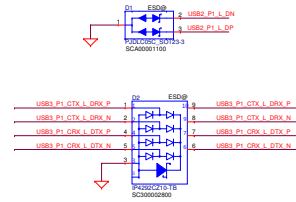
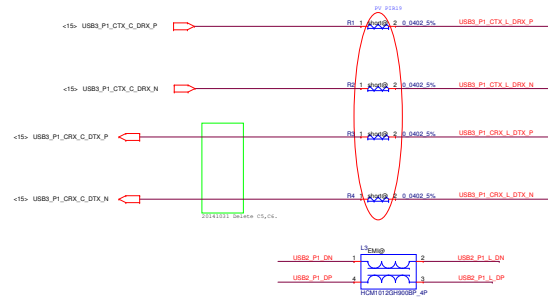
Place closed to JEDP1



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			Size C	Document Number	LA-C382P		Rev
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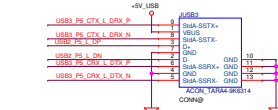
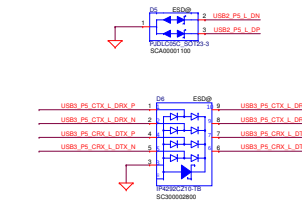
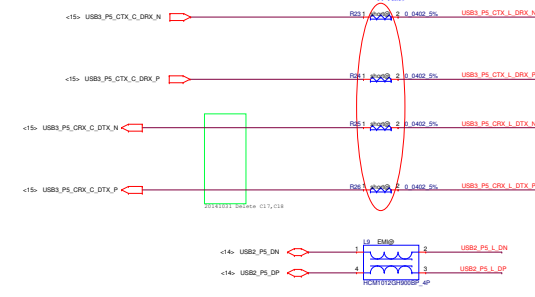
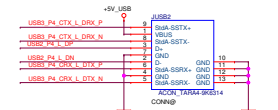
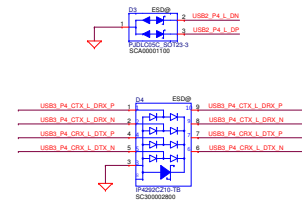
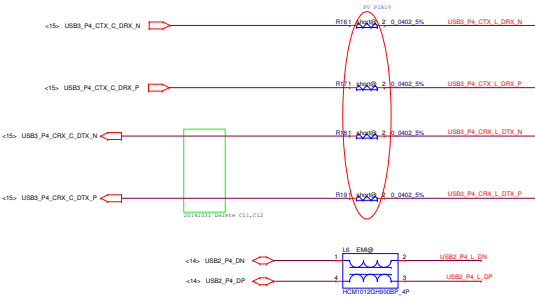
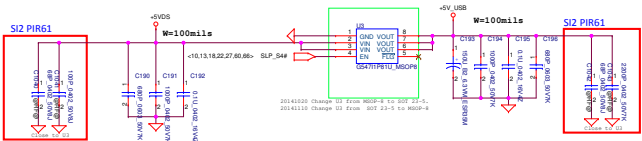
USB charger



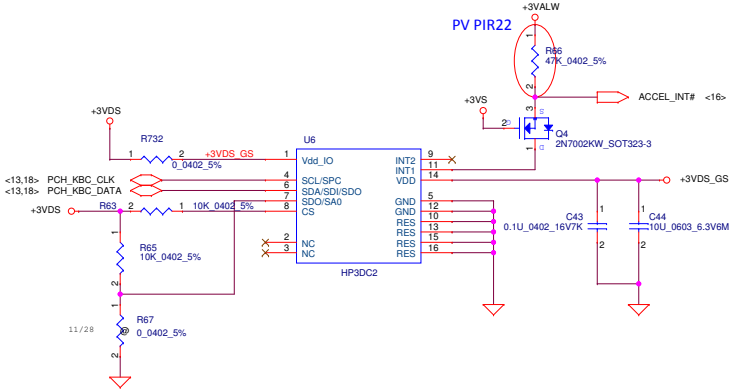
State	S0				S3, S4, S5			
Mode	CDP				DCP			
Control pin	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL
	1	1	1	1	0	0	1	1

CDP:Charging Downstream Port
DCP:Dedicated Charging Port

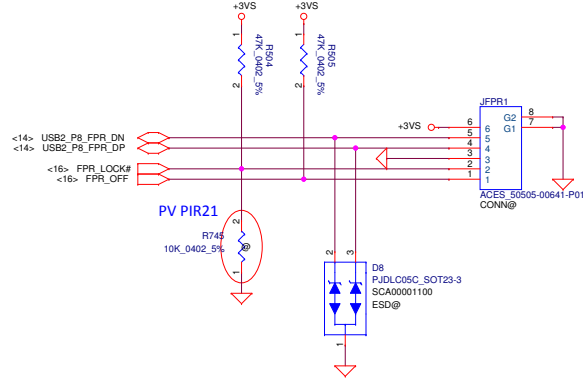
MB_USB 3.0 Without charger function



ACCELEROMETER

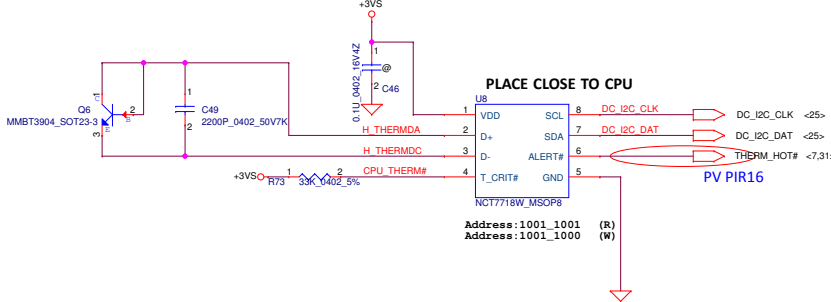


Finger printer

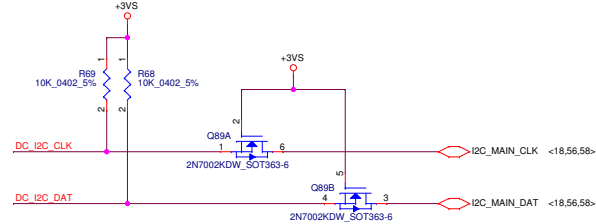
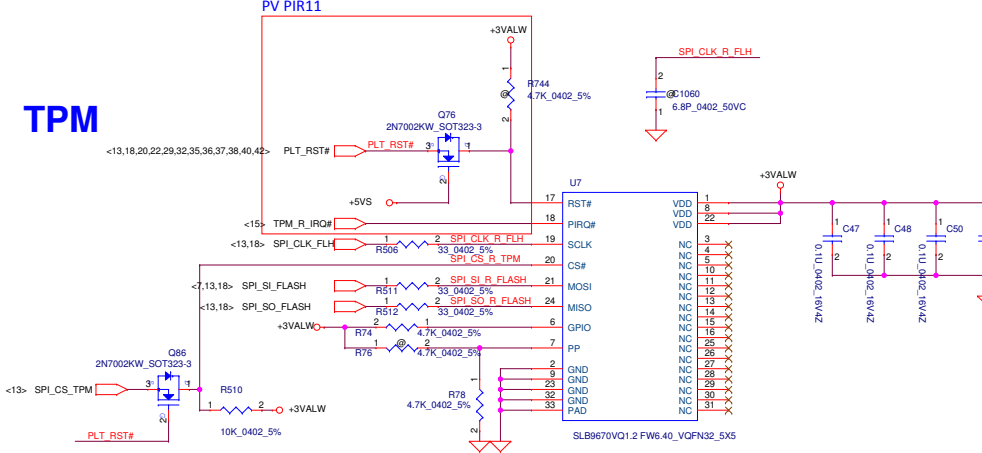


Vinafix.com

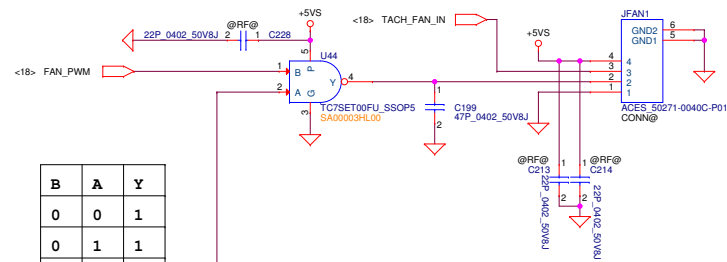
CPU THERMAL SENSOR



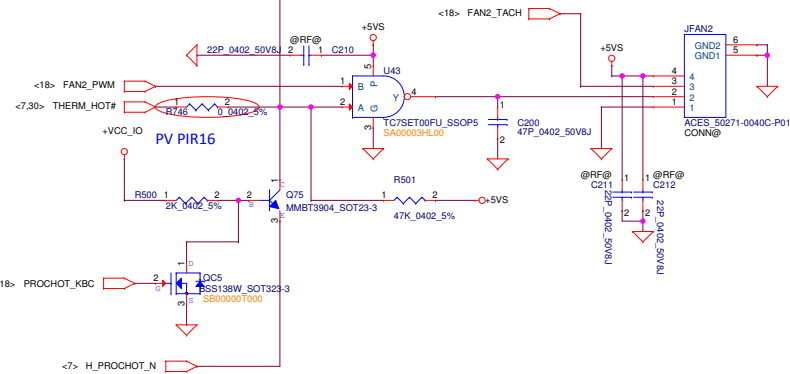
TPM



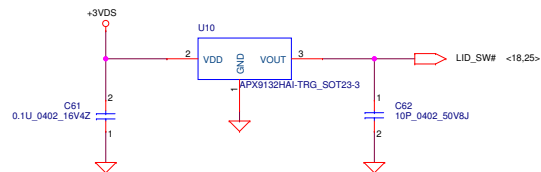
Fan Control Circuit



B	A	Y
0	0	1
0	1	1
1	0	1
1	1	0



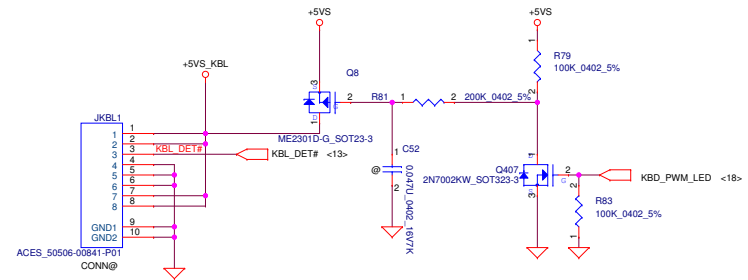
Lid Switch



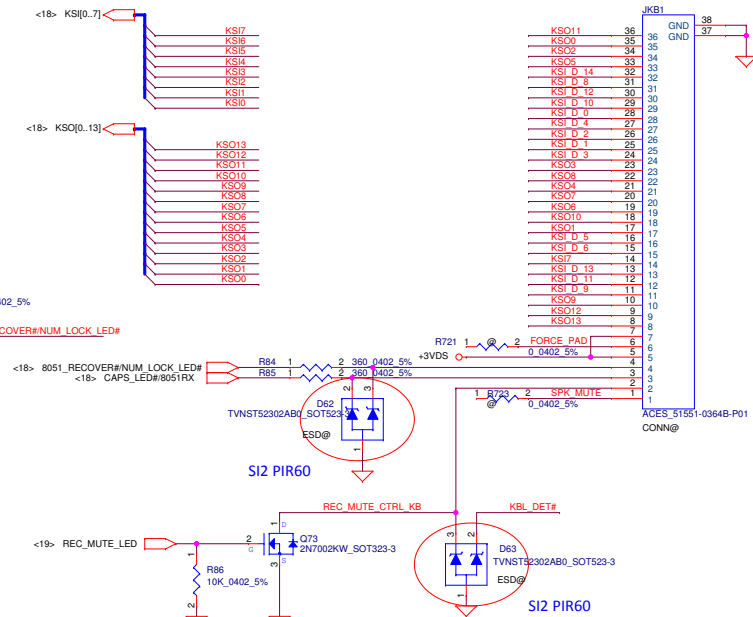
SI2 PIR 37

Remove R728/R729

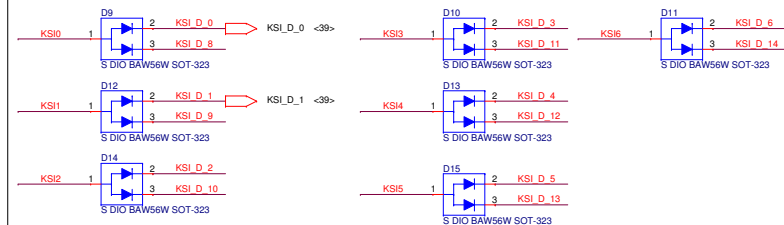
KB backlight Conn

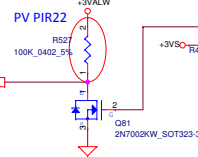
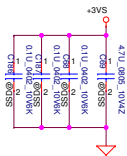


Keyboard conn



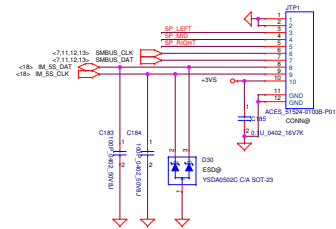
SI2 PIR60



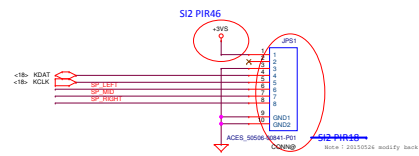


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TP/B TO M/B



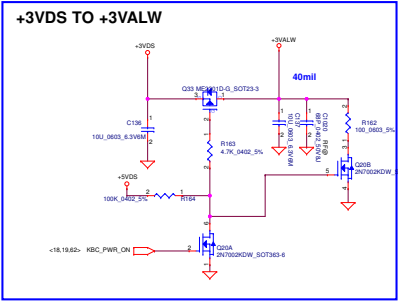
Stick Point



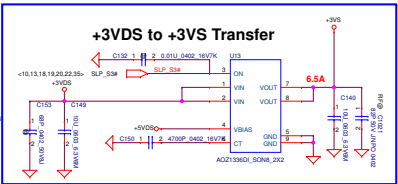
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Issued Date	2016/03/07	Deciphered Date	2018/03/07	
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Date: Issued: March 07, 2016				Page: 33 of 74

DC/DC

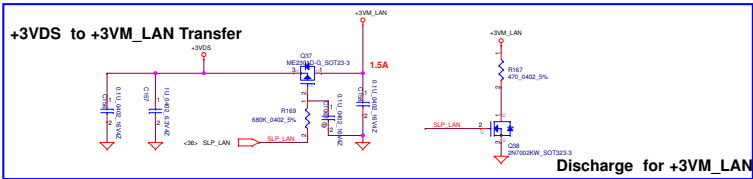
+3VDS TO +3VALW



+3VDS to +3VS Transfer

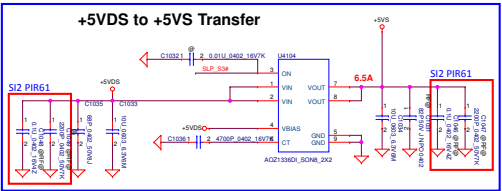


+3VDS to +3VM_LAN Transfer



Discharge for +3VM_LAN

+5VDS to +5VS Transfer

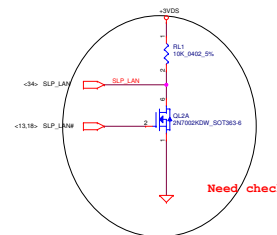
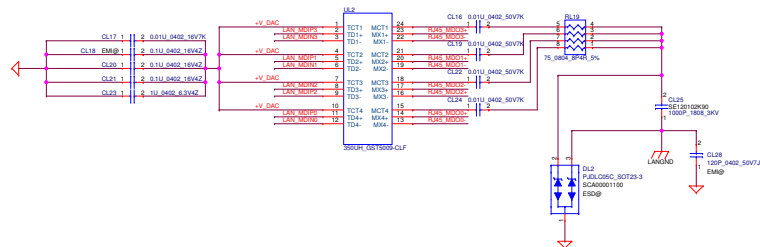
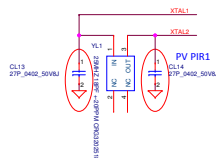
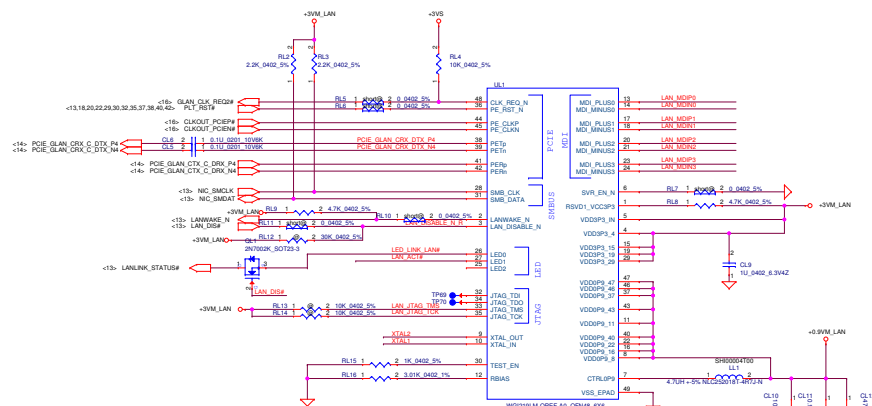
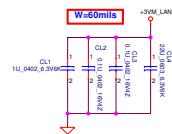




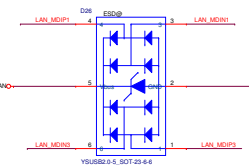
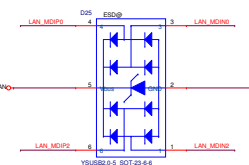
20141028 Add R530, R531, LED9, LED10 for D80 debug.

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Issued Date	2016/03/07	Deciphered Date	2018/03/07		
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JDATE: Monday, March 16, 2016					
JNAME: JPAGE: 35 OF 74					

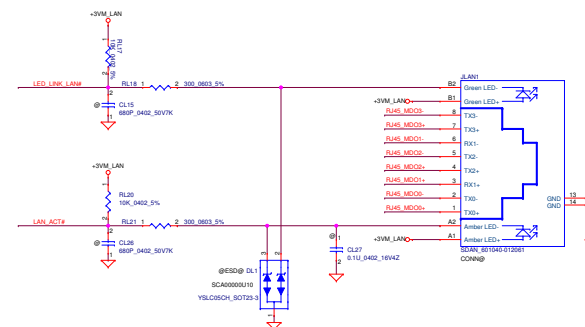
LAN



Need check

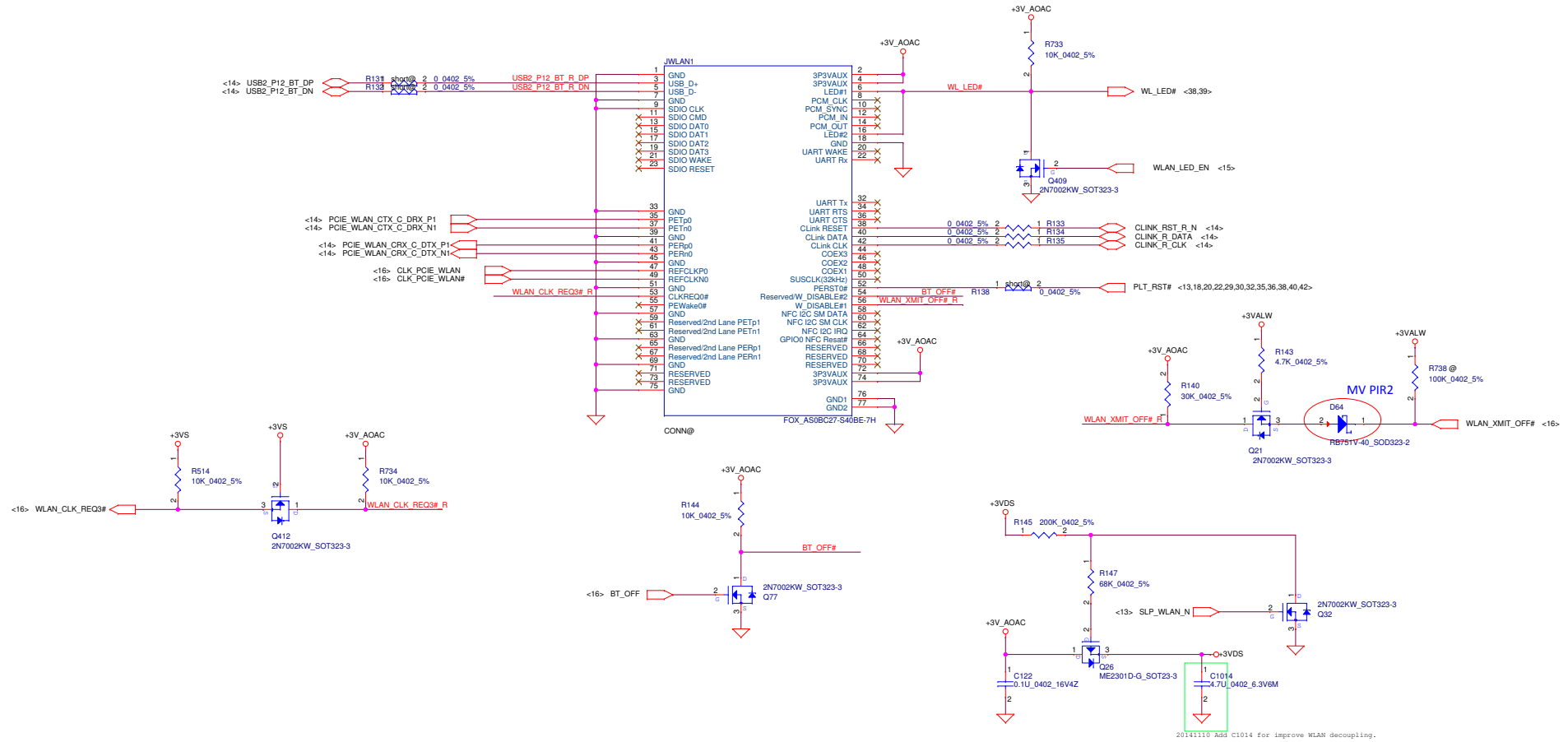


RJ-45 CONN.



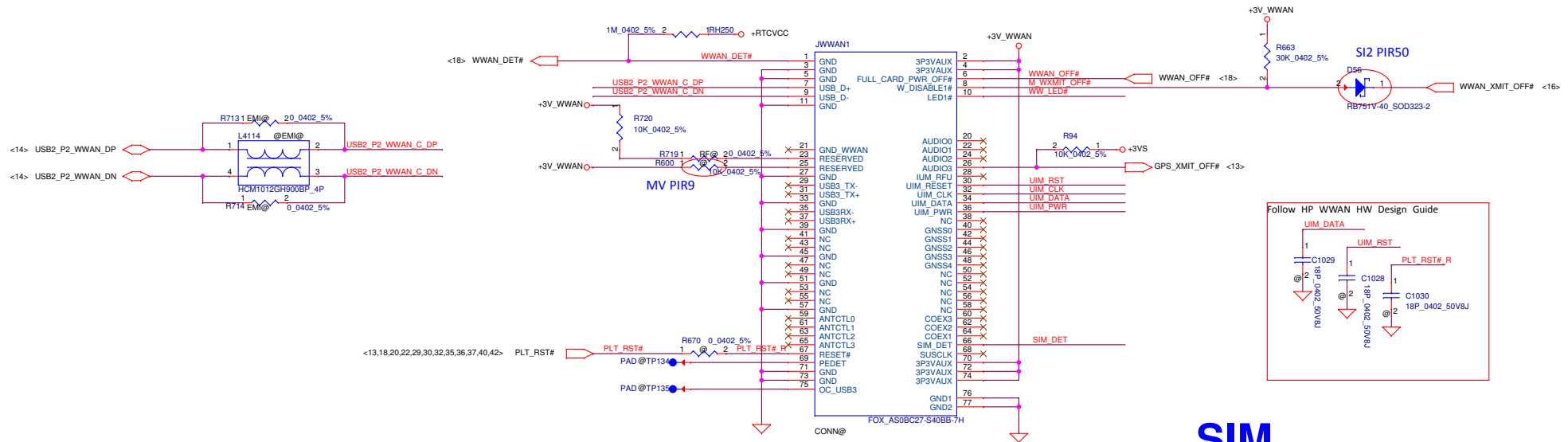
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DATE: 08/20/2018 BY: 60322 UCBAW/STW			Page 38 of 74

WLAN

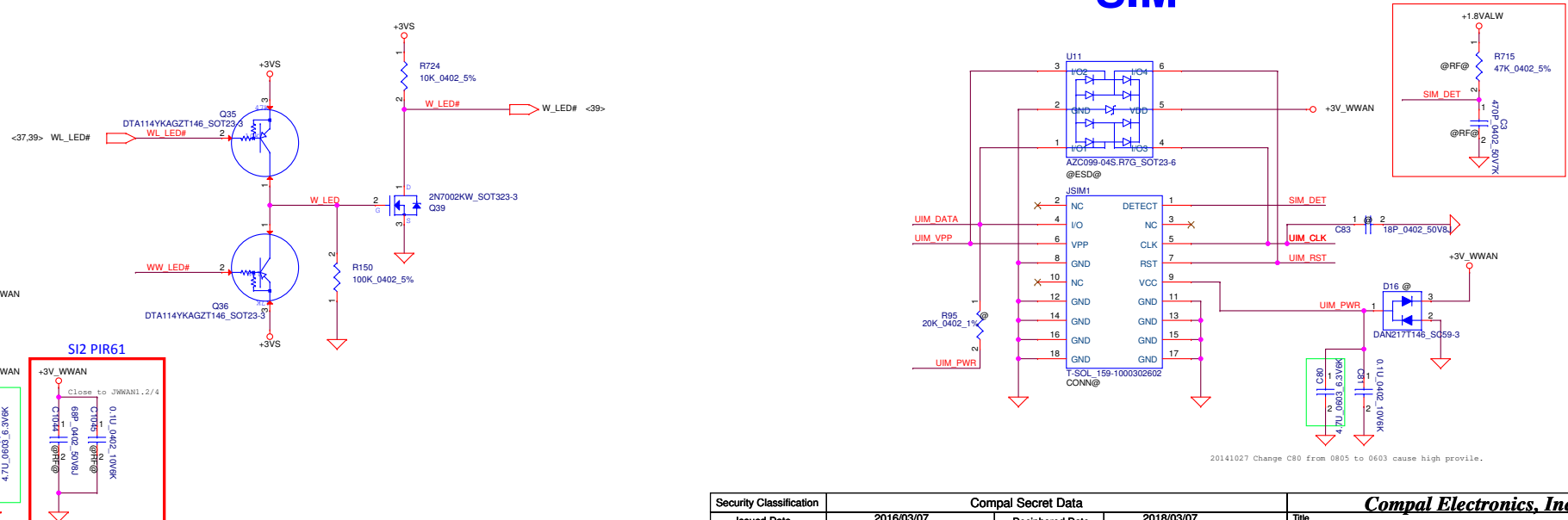


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				Date:	Tuesday, March 08, 2016	Sheet 37 of 74

WWAN



SIM

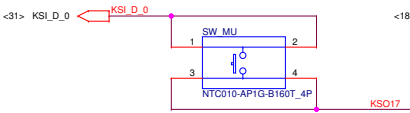


20141027 Change C80 from 0805 to 0603 cause high provile.

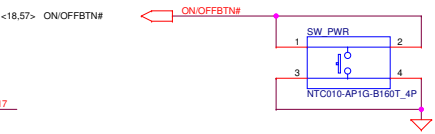
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				WWAN/SIM		
				Size	Document Number	Rev
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Wifi & mute Button

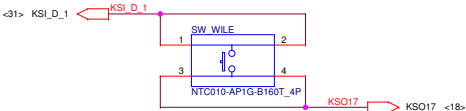
MUTE



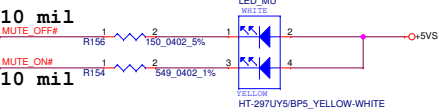
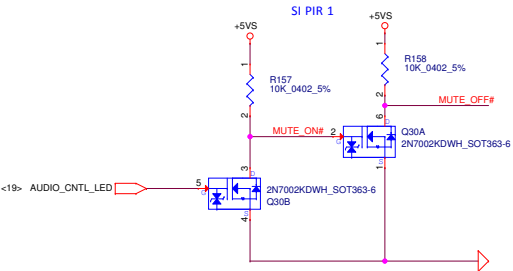
POWER Button



Wireless

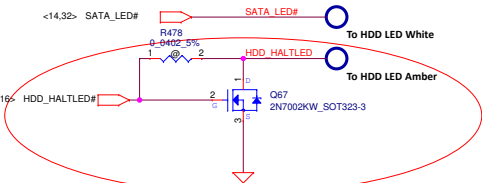


MUTE LED



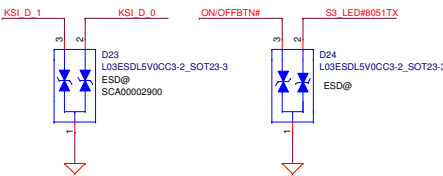
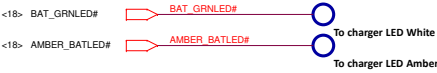
Connect to SB

HDD LED

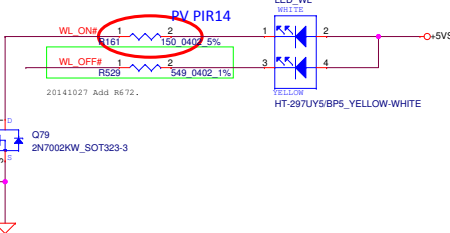


Charger LED

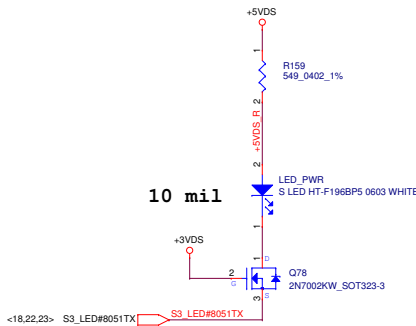
S12 PIR6



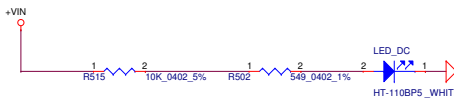
WLAN LED

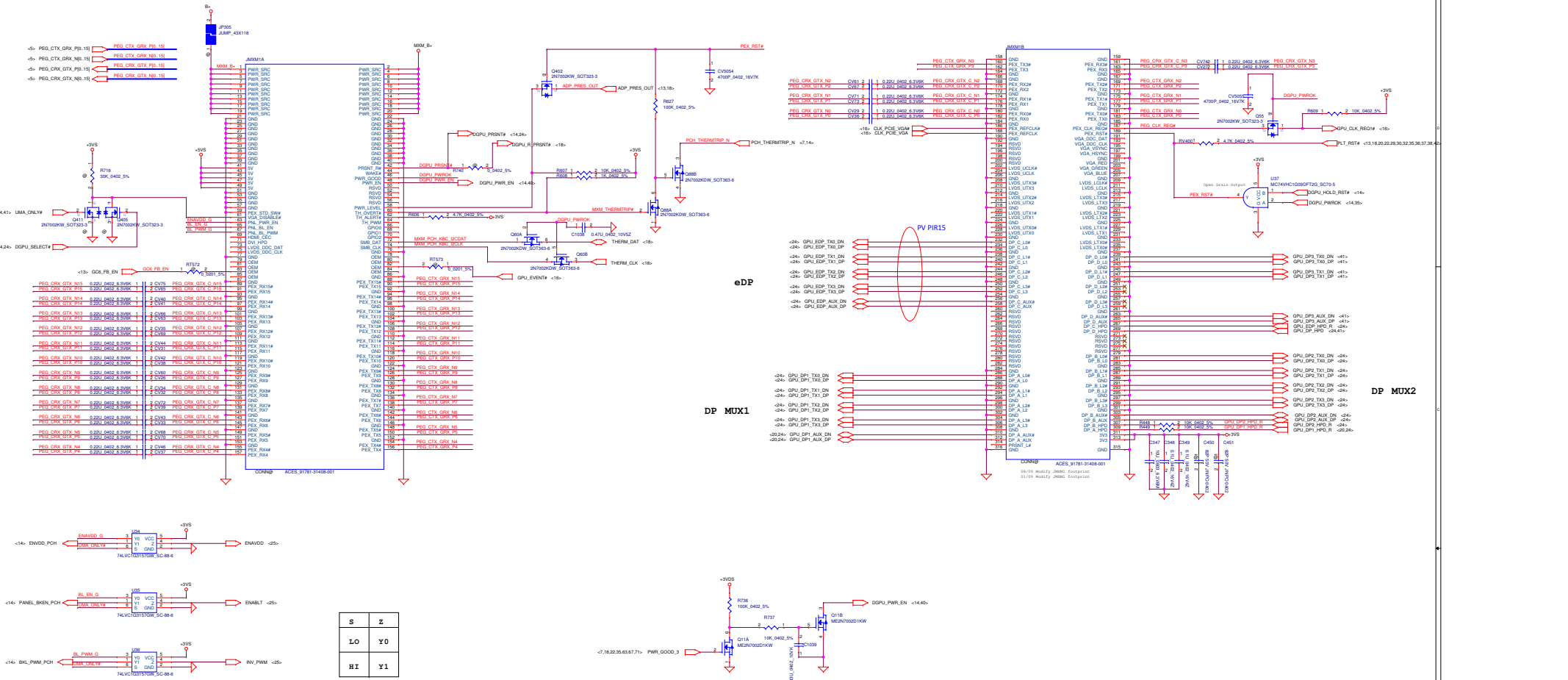


POWER LED



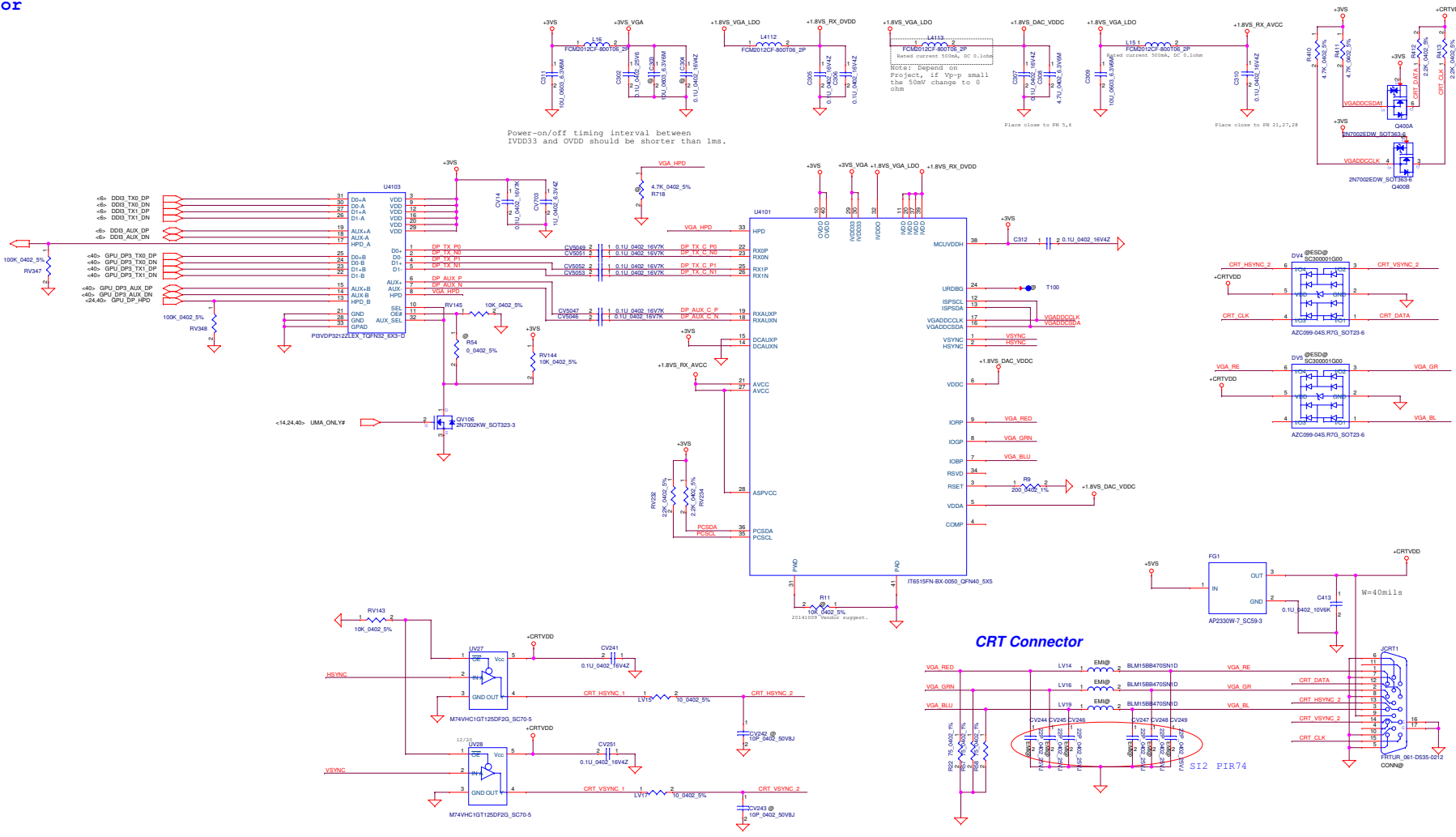
DC-IN LED



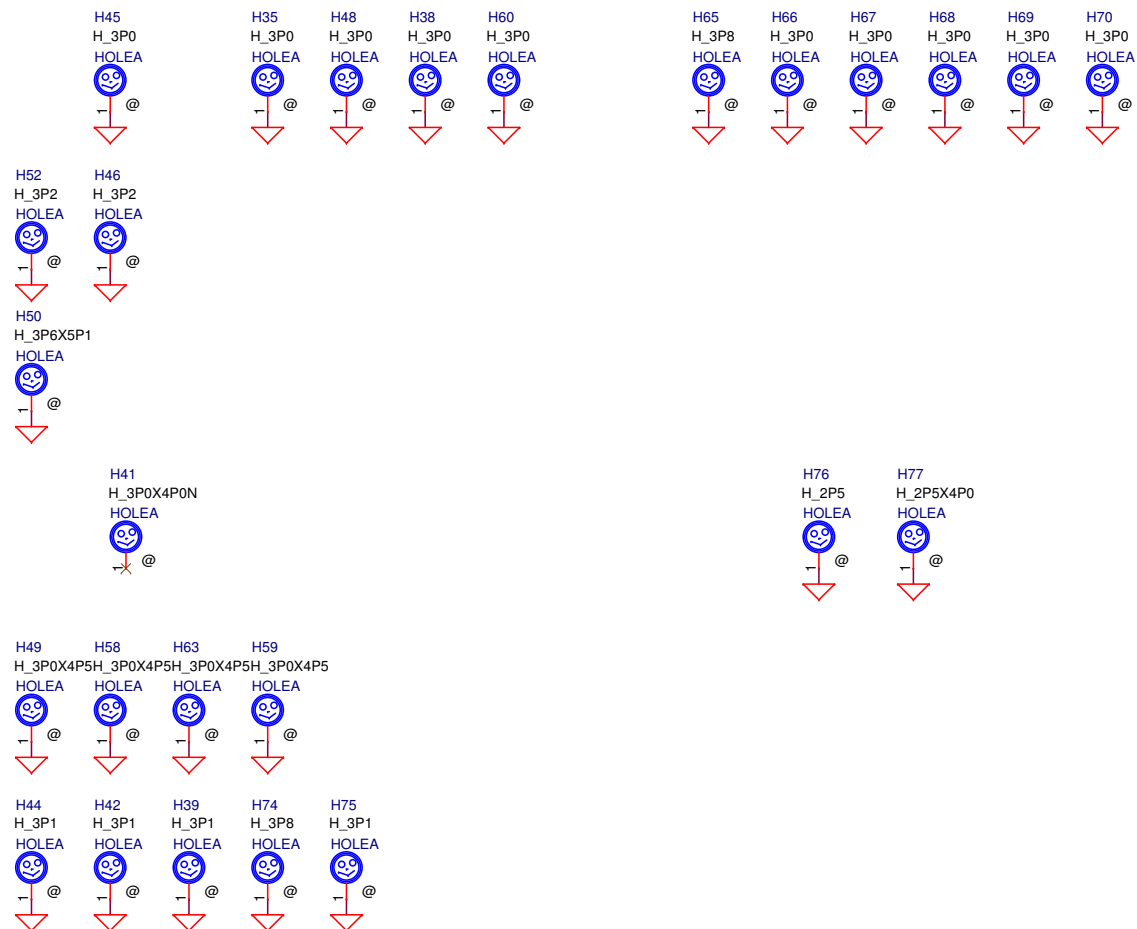
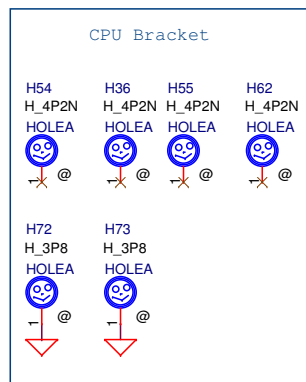
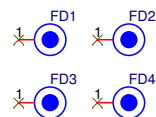


S	Z
LO	Y0
HI	Y1

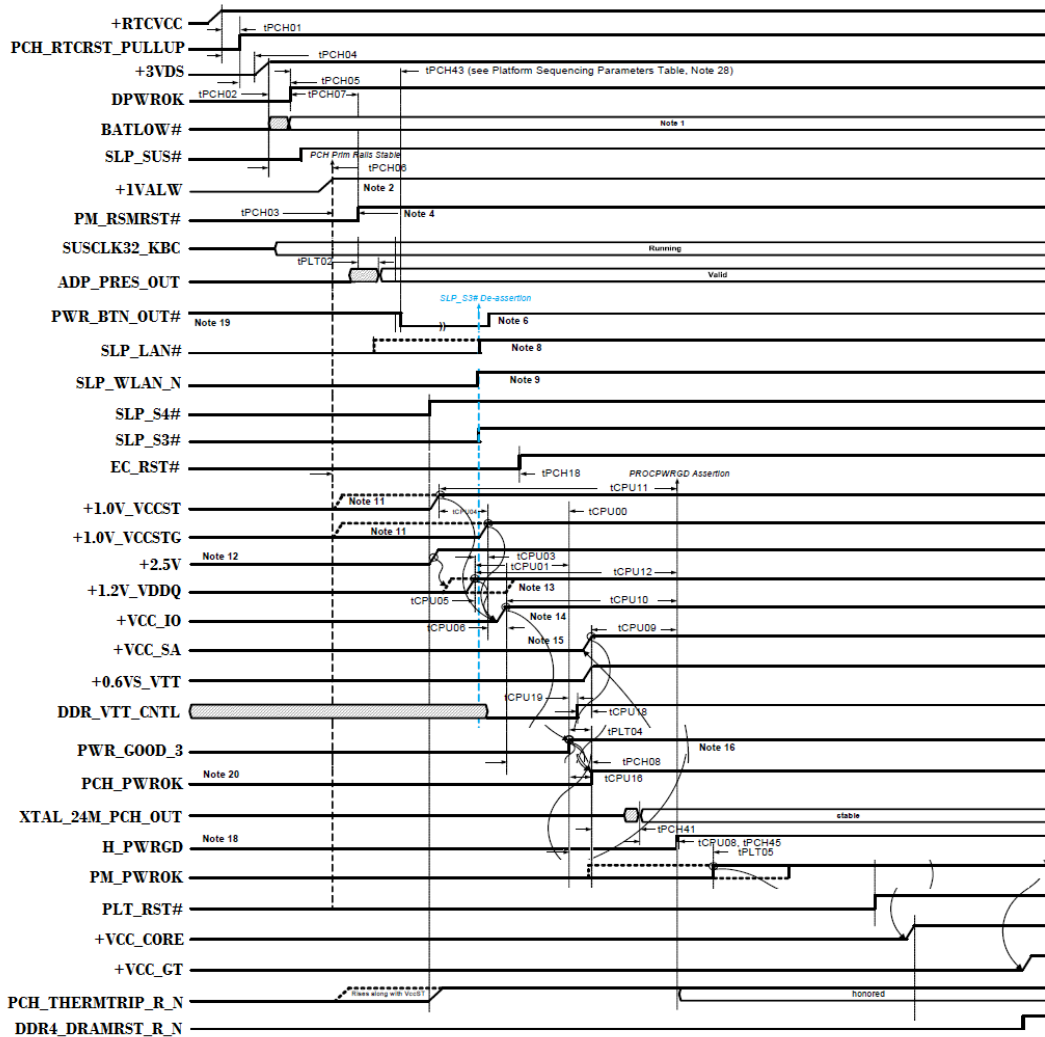
CRT BTB Connector



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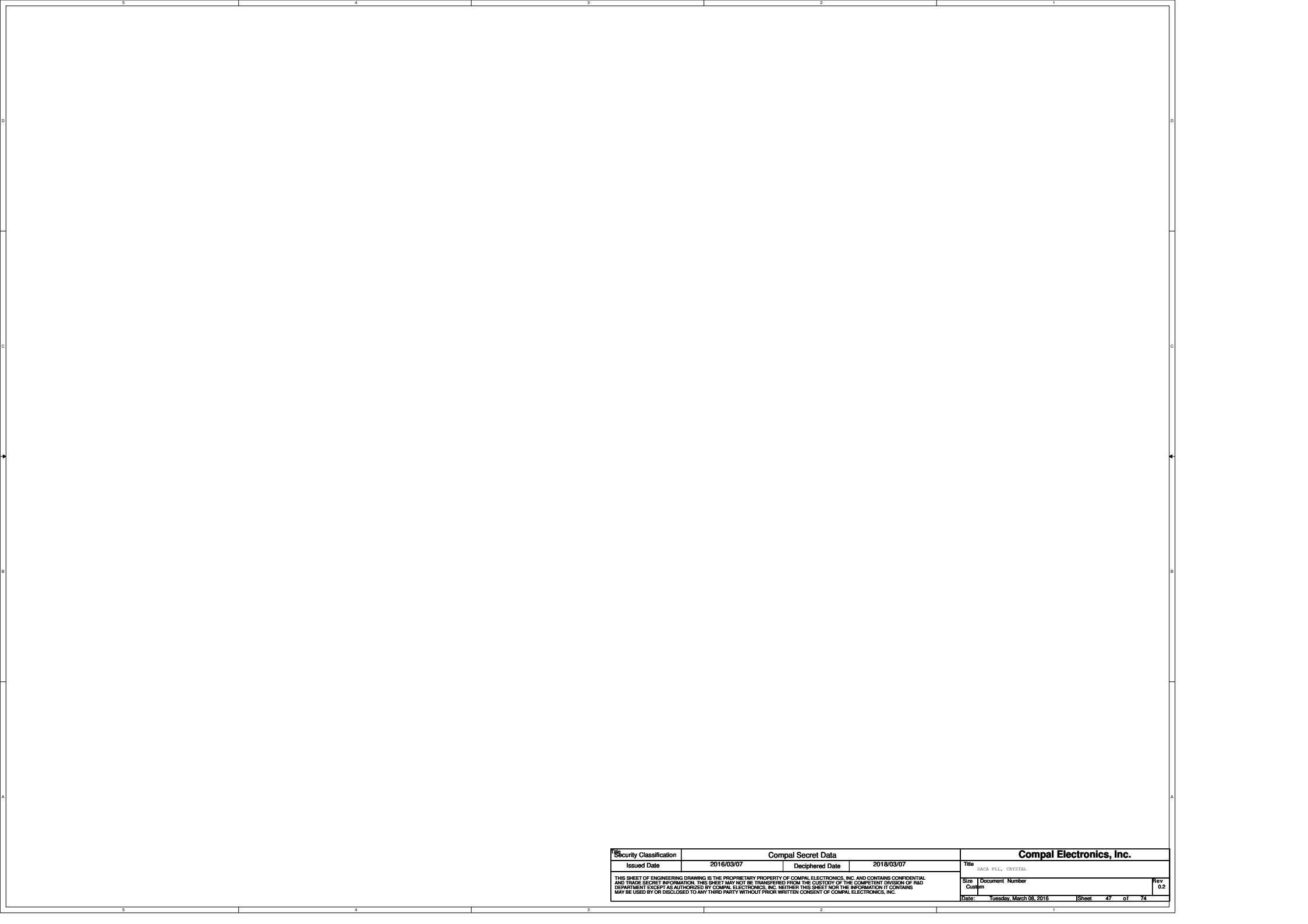


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Power Source name	Current (mA)
+RTCVCC	1
+3VDS	15100
+5VDS	39125
+1.8VALW	190
+1VALW	8183
+1.2V_VDDQ	14660
+1.0V_VCCST	265
+5VS	31625
+3VS	10846
+0.6VS_VTT	3000
+2.5VP	4000
+VCC_IO	5500
+VCC_GTX	20000
+VCC_SA	20000
+VCC_GT	20000
+VCC_CORE	20000

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Issued Date	2016/03/07	Deciphered Date	2018/03/07	Title UNCA PLL, CRYSTAL	
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				Date:	Tuesday, March 08, 2016	Sheet 49 of 74

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D				D																																				
C				C																																				
B				B																																				
A				A																																				
<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td>2016/03/07</td><td>Deciphered Date</td><td>2018/03/07</td><td colspan="2">Title</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Size Custom</td><td>Document Number</td></tr><tr><td colspan="4"></td><td>Date:</td><td>Tuesday, March 08, 2016</td></tr><tr><td colspan="4"></td><td>Sheet</td><td>51 of 74</td></tr><tr><td colspan="4"></td><td>Rev</td><td>0.2</td></tr></table>					Security Classification	Compal Secret Data			Compal Electronics, Inc.		Issued Date	2016/03/07	Deciphered Date	2018/03/07	Title		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number					Date:	Tuesday, March 08, 2016					Sheet	51 of 74					Rev	0.2
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Issued Date	2016/03/07	Deciphered Date	2018/03/07	Title																																				
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Install below X63 level BOM structure for ver. 0.1

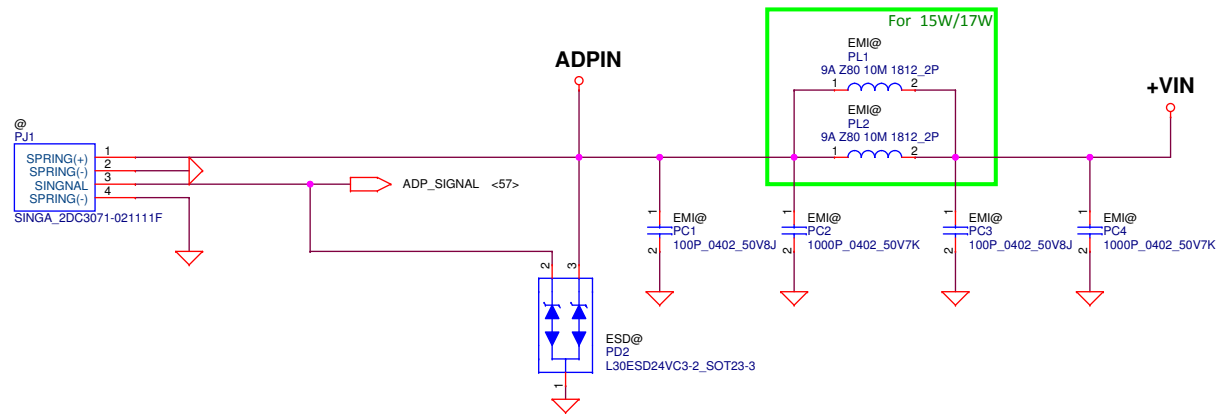
Un-pop parts BOM structure

- @ : reserve, un-pop on all sku
- @DIS@: Discrete sku parts, un-pop
- @DIS@EMI@ : Discrete sku parts and belong to EMI parts, un-pop
- @EMI@ : EMI parts, un-pop
- @H44e@ : CPU H44e sku parts, un-pop
- @H44e@EMI@ : CPU H44e sku parts and belong to EMI parts, un-pop

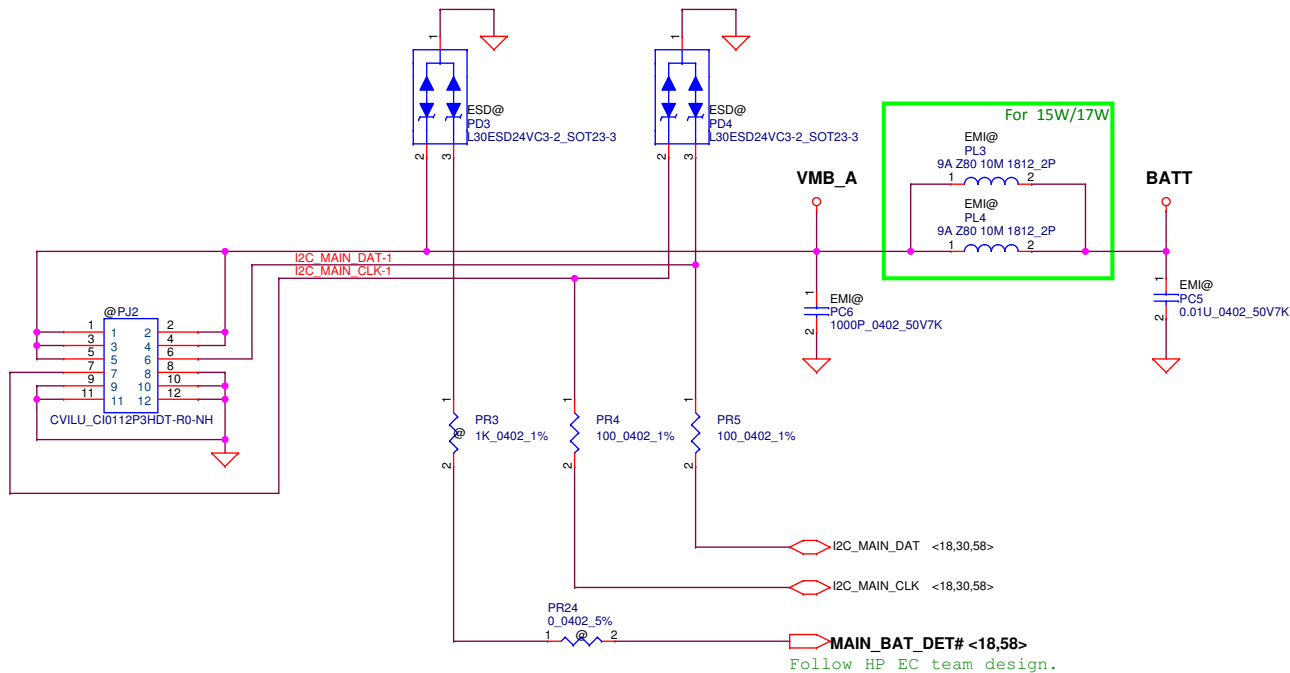
Pop parts BOM structure

- DIS@: Discrete sku parts, pop
- DIS@EMI@ : Discrete sku parts and belong to EMI parts, pop
- EMI@ : EMI parts, pop
- ESD@ : ESD parts, pop
- H42@ : pop on CPU H42 sku only
- H44e@ : pop on CPU H44e sku only
- H44e@EMI@ : EMI parts, pop on CPU H44e sku only

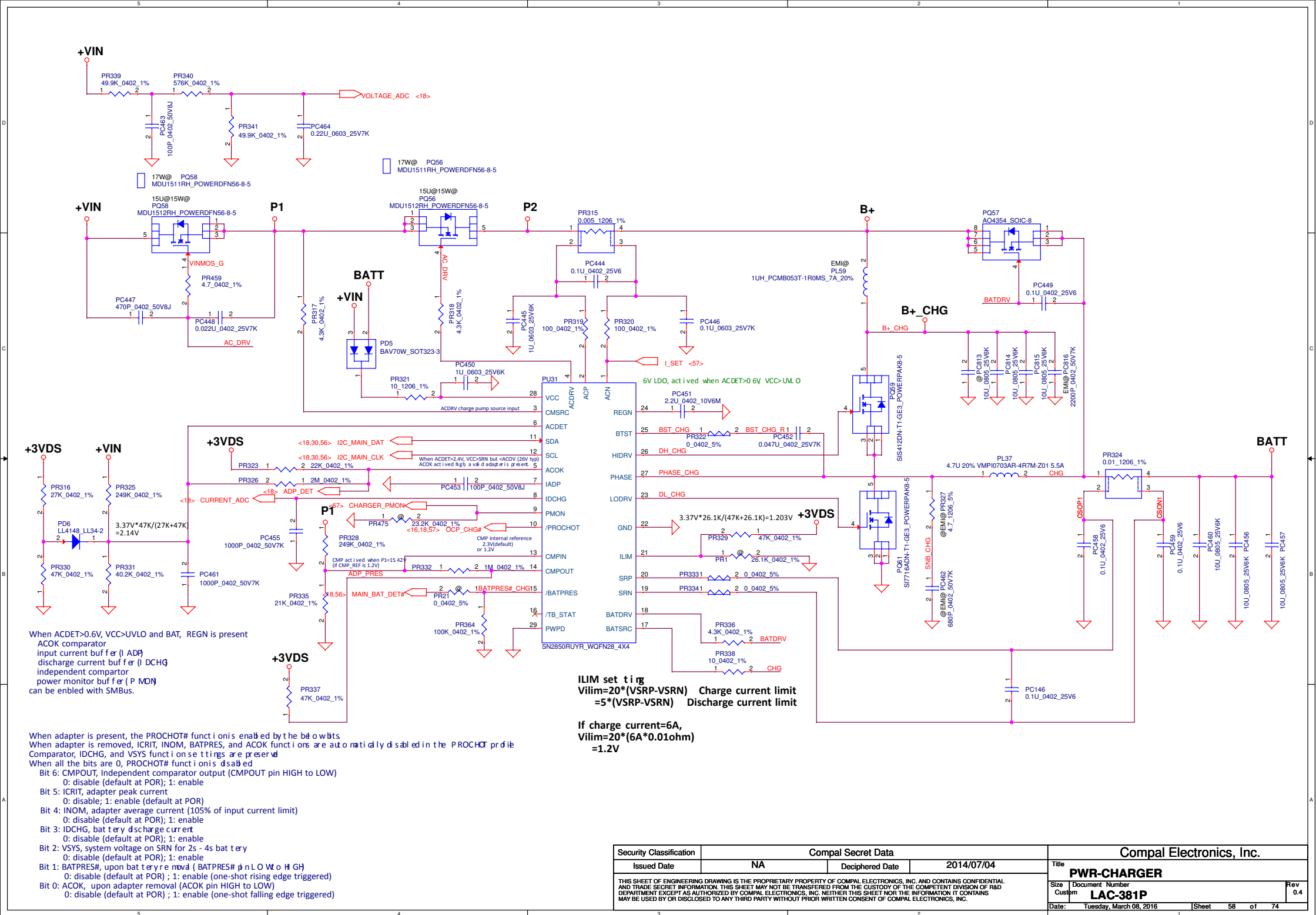
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					LAC-381P	0.4
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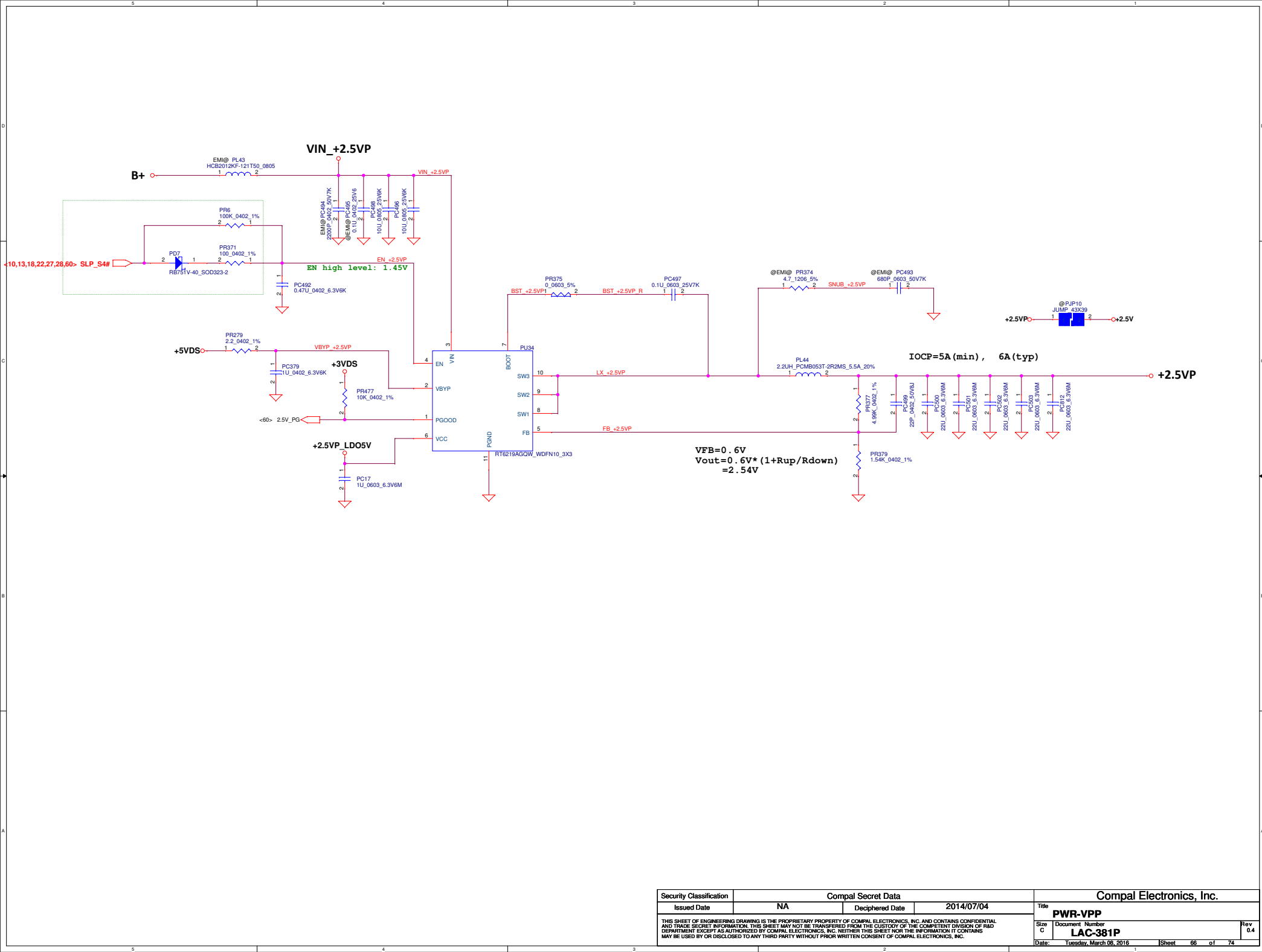


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				Size	Rev
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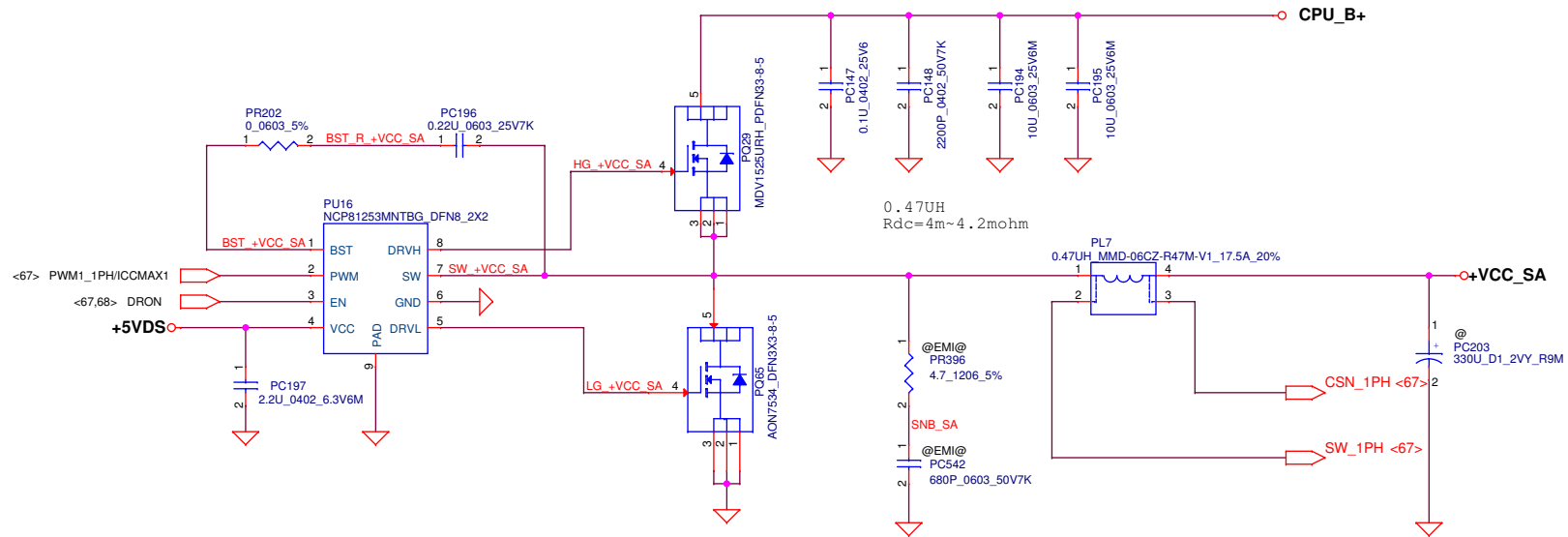


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Size		Document Number		Rev	
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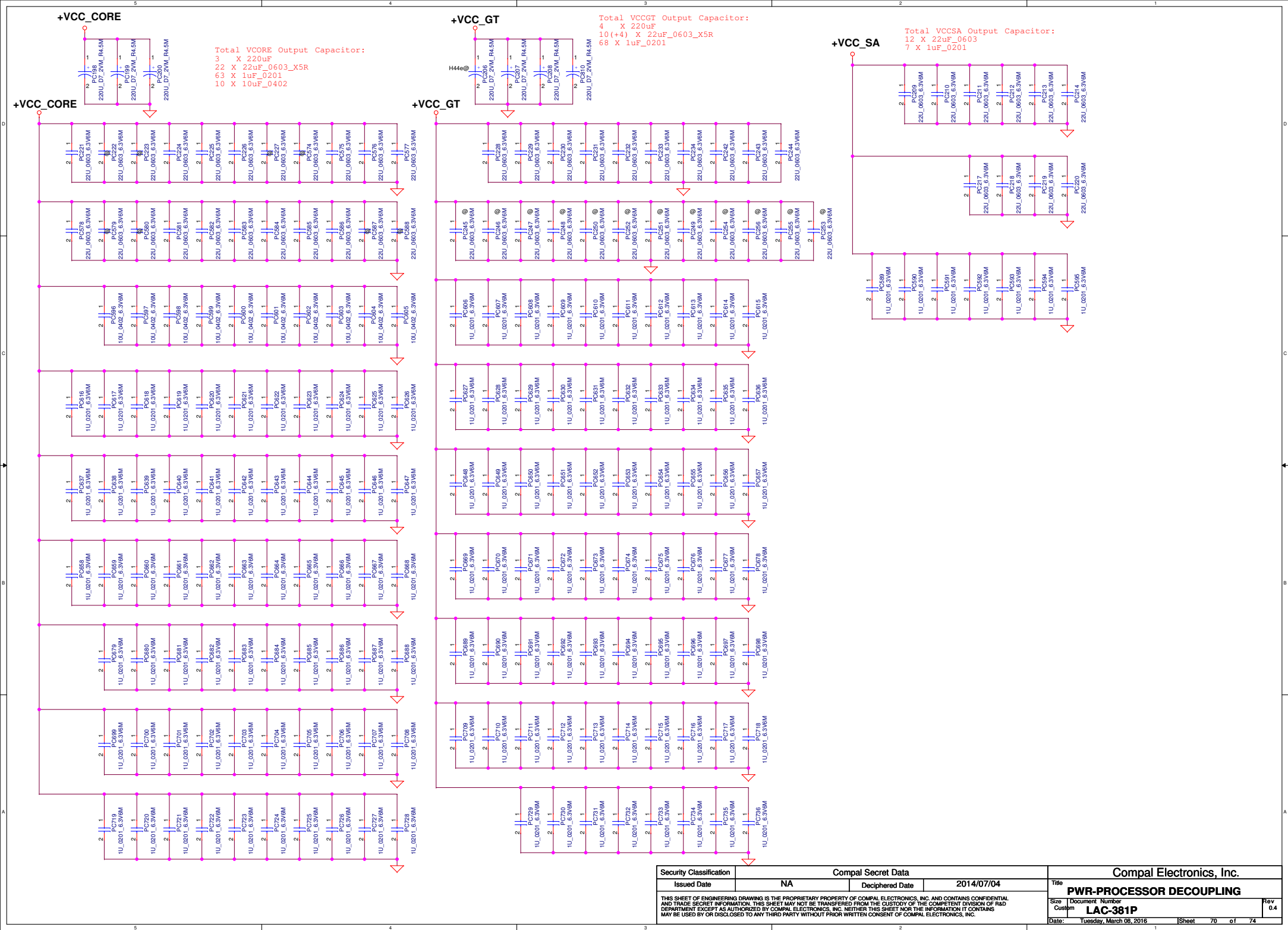




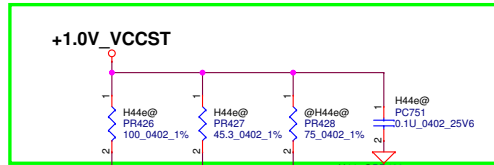
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				C	LAC-381P	0.4
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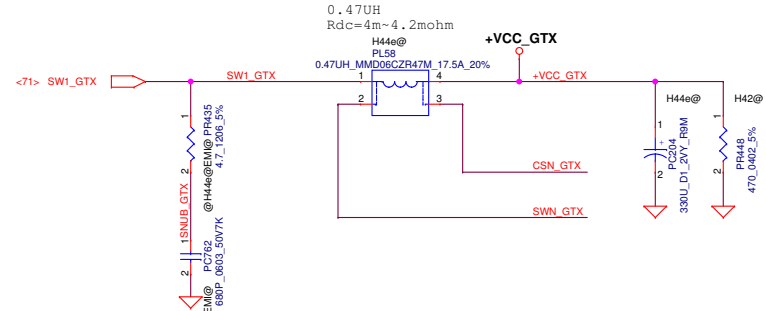
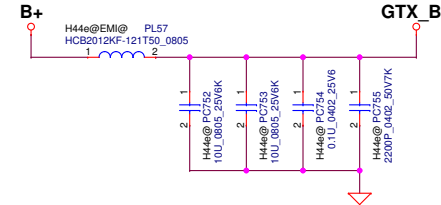
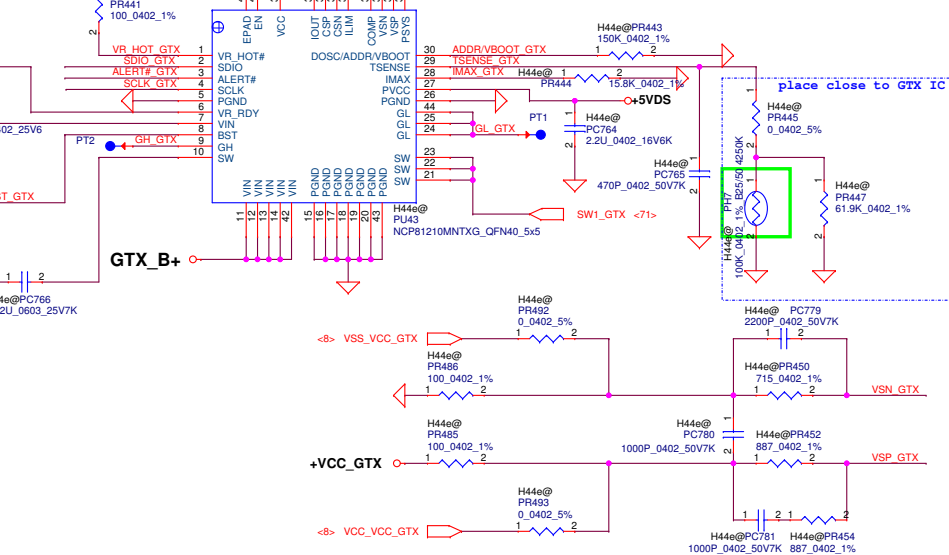
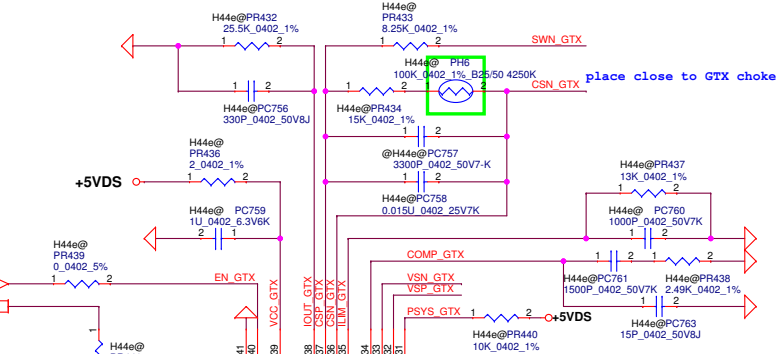
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It depend on NCP81206 or NCP81210 close to CPU will be unpop.

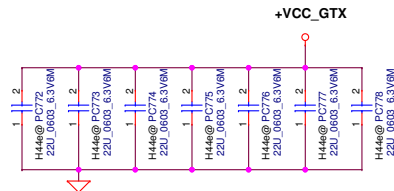


<7,67> SDIO GTX
<7,67> SCLK GTX
<7,67> ALERT# GTX

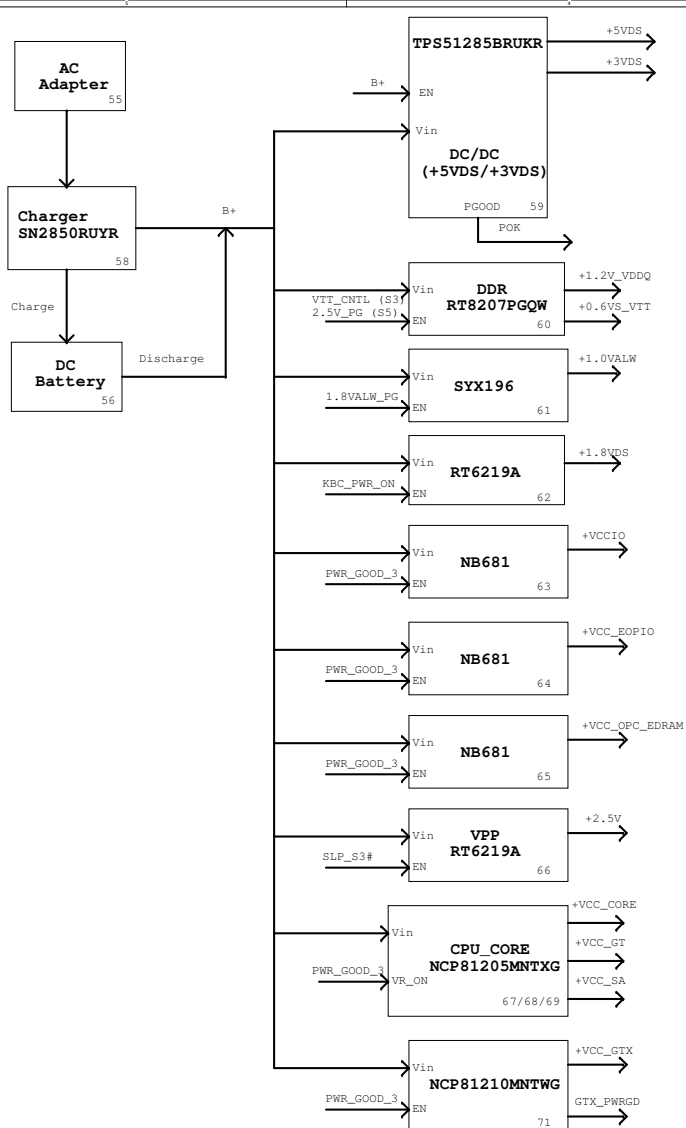


CPU spec: (SKL-H44e 45W)
VCCGTX: 9A
OCP Setting:
VCCGTX: 16.08A

output Capacitor:
6 X 22uF_0603_X5R * 12



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CPU DC/DC	
NCP81205MNTXG 67	
INPUTS	OUTPUTS
B+	+VCC_VORE +VCC_OT +VCC-SA
CPU DC/DC	
NCP81210MNTXG 71	
INPUTS	OUTPUTS
B+	+VCC-SA
SYSTEM DC/DC	
TPS81285B1RUKR 59	
INPUTS	OUTPUTS
B+	+VREG1/SVREG
SYSTEM DC/DC	
RT6219A 62	
INPUTS	OUTPUTS
B+	+1_VREG2
SYSTEM DC/DC	
SYX196 61	
INPUTS	OUTPUTS
B+	+1_0VALWE
SYSTEM DC/DC	
RTS207PGGW 60	
INPUTS	OUTPUTS
B+	+1_VCC_VORE +0_6VB_VTT
SYSTEM DC/DC	
NE661 63	
INPUTS	OUTPUTS
B+	+VCC1D
SYSTEM DC/DC	
NE661 64	
INPUTS	OUTPUTS
B+	+VCC_EOP1D
SYSTEM DC/DC	
NE661 65	
INPUTS	OUTPUTS
B+	+VCC_OPC_DORAR
SYSTEM DC/DC	
RT6219A 66	
INPUTS	OUTPUTS
B+	+2_0VB
CHARGER	
SN2850RU0YK 58	
INPUTS	OUTPUTS
BATT	
Switches 7	
INPUTS	OUTPUTS

**Version change list
(P.I.R. List)**

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for PWR**

Item	Reason for change	PG#	Modify List	Date	Phase
1	1. Power button delay circuit by customer requirement. 2. VCC_CORE current balance control by vendor requirement. 3. For VCORE input by vendor requirement.	#57 #65 #66 #67 #69	1. Add PU8, PH1, PC106, PR111, PC104, PR107, PC107, PR113, PR112, PR103, PR101, PQ16, PR460, PR461, PC739, PQ19 2. Add I97, PR198, PR199 3. Add PC147, PC148, PC149, PC150, PC151, PC 152, PC153, PC154, PC155, PC156, PC157, PC158, PC159, PC160 0.1uF & 2200pF Change PC754, PC755 to 0.1uF & 2200pF	2014/11/06	DB0
2	1. IMAx calculation of NCP81210 changed. 2. Delay +1VALW by customer requirement. 3. Modify 1.8V net name by customer requirement.	#69 #61 #62	1. Change PR444 to 10K. 2. Change PR410 to 4.7K, PC16 to 0.01uF. 3. Change +1.8VDS to +1.8VALW.	2014/11/14	DB0
3	1. Update PG net name of 3V/5V, DDR, 2.5V, VCC/VCCGTX. 2. Modify DDR PG circuit. 3. Modify VCCIO enable/PG circuit. 4. Add pull low resistance at +VCC_GTX for SKL-H42.	#59~#69 #60 #63 #69	1. Modify PG 3V/5V to "VDS_PG", 2.5V to "2.5V_PG". VCC/VCCGTX to "VR_PWROK". 2. Change PU4 to MCT4VHCIG09DFT2G, add PR91 100 ohm. 3. Add PR281 10K ohm, PR280, PR282, PR283 0 ohm. 4. Add PR448 470ohm.	2014/11/17	DB0
4	1. Changing to improve efficiency. 2. To meet INTEL requirement.	#60 #62, #66 #61 #64, #65	1. Change PL11 from 1.5uH to 1uH. 2. Change PL42, PL44 size to 5x5x3mm. 3. Change +1.0VALW solution from TP551212 to SYX196, Add 2xNB681 for +VCC_EOPIO & +VCC_OPC_EDRAM.	2014/12/22	DB1
5	Fine tune Vcore compensation	#67	1. Change PR120 from 1.4k ohm to 1.69k ohm. 2. Change PC110 from 1000pF to 3300pF. 3. Change PC116 from 0.015uF to 8200pF. 4. Change PR127 from 28.7k ohm to 48.7k ohm. 5. Change PR145 from 22.6k ohm to 23.2k ohm. 6. Change PC131 from 1000pF to 820pF. 7. Change PR169 BOM Structure from H42@ to @H42@. 8. Change PR177 BOM Structure to @H42@. 9. Change PR164 from 75k ohm to 80.6k ohm. 10. Change PR166 from 75k ohm to 80.6k ohm. 11. Change PR189 BOM Structure to @H42@. 12. Change PC145 BOM Structure to @H42@. 13. Change PR193 BOM Structure from @ to H44e@. 14. Change PR181 from 24.9K ohm to 169K ohm.	2015/01/05	DB1
6	1. Power control 2. Fine tune 2.5V leakage power 3. Fine tune Vcore compensation	#64, #65 #66 #67~#69	1. Add EOPIO/EDRAM control circuit. 2. Change PR377 from 47.5K ohm to 4.99K ohm, PR379 from 15K ohm to 1.54Kohm. 3. Change PR138 from 1Kohm to 357ohm, PR155 from 16.2Kohm to 16.9Kohm. Change PR146, PR153 from 4.7Kohm to 3Kohm, PC124, PC129 from 2200pF to 3300pF. Change PC132, PC135 from 0.01uF to 0.1uF. Change PC110 from 3300pF to 5600pF. Change PR380, PR381, PR390, PR391, PR400, PR401 from 0ohm to 3.9ohm.	2015/01/14	DB1
7	1. Modifying for battery MAIN_BAT_DET# signal. 2. fine tune Vcore compensation.	#56 #67	1. Change PR364 from 0 ohm to 100K ohm. 2. Change PR120 to 1.78K ohm, PR138 to 681K ohm, PR151 to 23.2K ohm.	2015/03/30	SI1
8	Change 3V/5V MOSFET.	#59	Change 3V/5V MOSFET from C5D87381 to TPN11003NL + AON7534.	2015/06/09	SI2
9	Reduce 1.8V voltage leakage.	#62	Change PR368 to 4.99Kohm, PR370 to 2.49K ohm.	2015/06/09	SI2
10	Update schematic for CPU H4+4e.	#67	Update BOM structure for PR177, PR189, PC145	2015/06/26	SI2
11	1. To improve response time for PMON 2. Modifying the enable circuit by customer requirement. 3. For 3V/5V high side MOS 2nd source. 4. Chage 0 ohm to short PAD.	#58 #60, #66 #59 #57~#67	Change PR333, PR334 from 10 ohm to 0 ohm Add PD7, PD8, PD9 RB751 diode Change PQ68, PQ70 to AON7506 Change PR159, PR322, PR333, PR334, PR357, PR356, PR363, PR360, PR18, PR366, PR411, PR375, PR132, PR136, PR139, PR142, PR128 to short PAD.	2015/08/11	PV
12	1. Modify long press PWR_BTN circuit by customer required. 1. Modify CPU/GTX transient for CPU H44e.	#57 #67, #71	1. Change PR461 to 1M, add PR462, PR463 931K. 2. Change PR432 to 25.5K, PR444 to 15.8K, PR120 to 866, PR145 to 22.1K, PR154 to 13.7K, PR147 to 549, PR127 to 63.4K, PR134 to 24.9K, PR151 to 22.1K, PR155 to 14.7K, PR152 to 549, PR175 to 73.2K, PR179 to 59K,	2015/08/26	PV
13	Add RF cap	#72	Install PC858, PC863, PC871, PC872, PC467, PC875, PC873, PC878, PC876, PC880, PC881, PC882, PC869, PC868, PC870	2015/08/27	PV
14	Modify OTP setting to 65C act.	#57	Changing PR111 to 41.2K ohm, PR103 to 100K ohm, PR101 to 215K ohm.	2015/11/05	TLD
14	Modify RT8219A OCP setting from 7.44A to 8.4A. (worst case)	#57	Changing PR47 from 9.76K to 11.3K ohm.	2016/01/04	MV

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